# MIPI® DSI BRIDGE to eDP

**Check for Samples: SN65DSI86 , SN65DSI96**

## FEATURES

- **Embedded DisplayPort (eDP) 1.4 Compliant Supporting 1, 2, or 4 Lanes at 1.62Gbps (RBR), 2.7Gbps (HBR), or 5.4Gbps (HBR2).**
- **Implements MIPI® D-PHY Version 1.1 Physical Layer Front-End and Display Serial Interface (DSI) Version 1.02.00**
- **Dual Channel DSI Receiver Configurable for One, Two, Three, or Four D-PHY Data Lanes Per Channel Operating up to 1.5Gbps Per Lane**
- **Supports 18 bpp and 24 bpp DSI Video Packets with RGB666 and RGB888 Formats**
- **Suitable for 60fps 4K 4096x2304 Resolution at 18bpp Color, and WUXGA 1920x1200 Resolution with 3D Graphics at 60fps (120fps Equivalent)**
- **MIPI® Front-End Configurable for Single-Channel or Dual-Channel DSI Configuration**
- **Supports Dual Channel DSI ODD/EVEN and LEFT/RIGHT Operating Modes**
- **1.2V Main VCC Power Supply and 1.8V supply for Digital I/Os**
- **Low Power Features Include Panel Refresh and MIPI® Ultra-Low Power State (ULPS) Support**
- **DisplayPort Lane Polarity and assignment configurable.**
- **Supports 12MHz, 19.2MHz, 26MHz, 27MHz, and 38.4MHz REFCLK**
- **Adaptive content management and backlight PWM control enabling optimal user viewing experience in both low and bright ambient light environments available in SN65DSI96.**
- **ESD Rating ±4 kV (HBM)**
- **Packaged in 64-pin 5x5mm PBGA (ZQE)**
- **Temperature Range: –40°C to 85°C**

## APPLICATIONS

- **Tablet PC, Notebook PC, Netbooks**
- **Mobile Internet Devices**


## DESCRIPTION

The SN65DSI86/96 DSI to embedded DisplayPort (eDP) bridge features a dual-channel MIPI® D-PHY receiver front-end configuration with 4 lanes per channel operating at 1.5Gbps per lane; a maximum input bandwidth of 12Gbps. The bridge decodes MIPI® DSI 18bpp RGB666 and 24bpp RGB888 packets and converts the formatted video data stream to a DisplayPort with up to four lanes at either 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, or 5.4Gbps.

The SN65DSI86/96 is well suited for WQXGA at 60 frames per second, as well as 3D Graphics at 4K and True HD (1920x1080) resolutions at an equivalent 120fps with up to 24 bits-per-pixel. Partial line buffering is implemented to accommodate the data stream mismatch between the DSI and DisplayPort interfaces.

Integrated into the SN65DSI96 is an adaptive content management and backlight PWM control called *Assertive Display*. The *Assertive Display* core's purpose is to optimize the viewing experience on a multimedia display as a function of viewing environment. It provides coherent management of the multimedia viewing experience from total darkness to bright ambient light conditions enabling the display to operate at reduced power and in bright sunshine.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

Designed with industry compliant interface technology, the SN65DSI86/96 is compatible with a wide range of micro-processors, and is designed with a range of power management features including Panel Refresh Support, and the MIPI® defined ultra-low power state (ULPS) support.

The SN65DSI86/96 is implemented in a small outline 5x5mm PGBA at 0.5mm pitch package, and operates across a temperature range from –40°C to 85°C.

In the rest of this document, the SN65DSI86/96 will be referred to as SN65DSIX6. Anytime SN65DSI86 or SN65DSI96 is used then that particular sentence and/or feature only refers to that specific part.

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### FUNCTIONAL DESCRIPTION

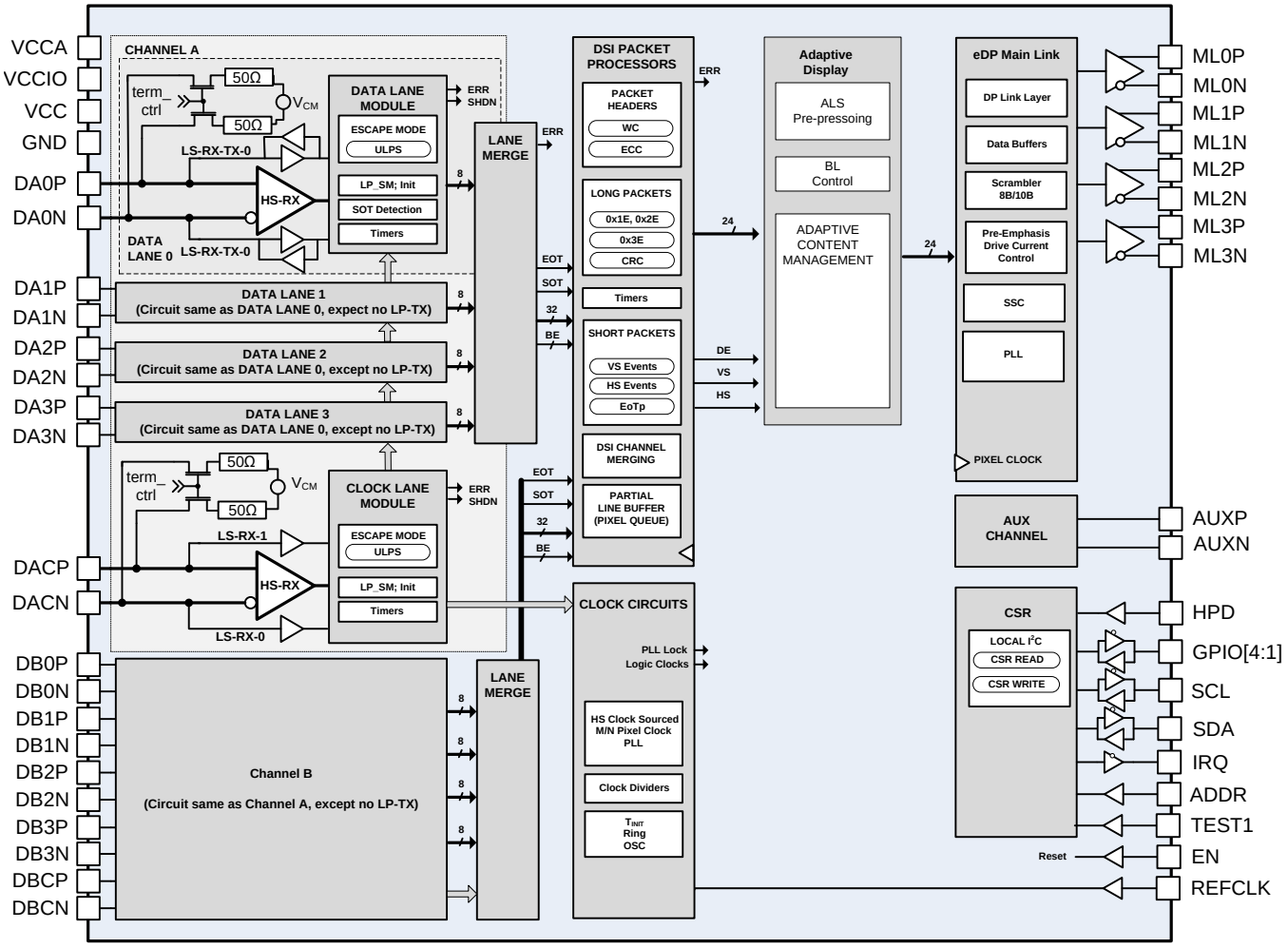
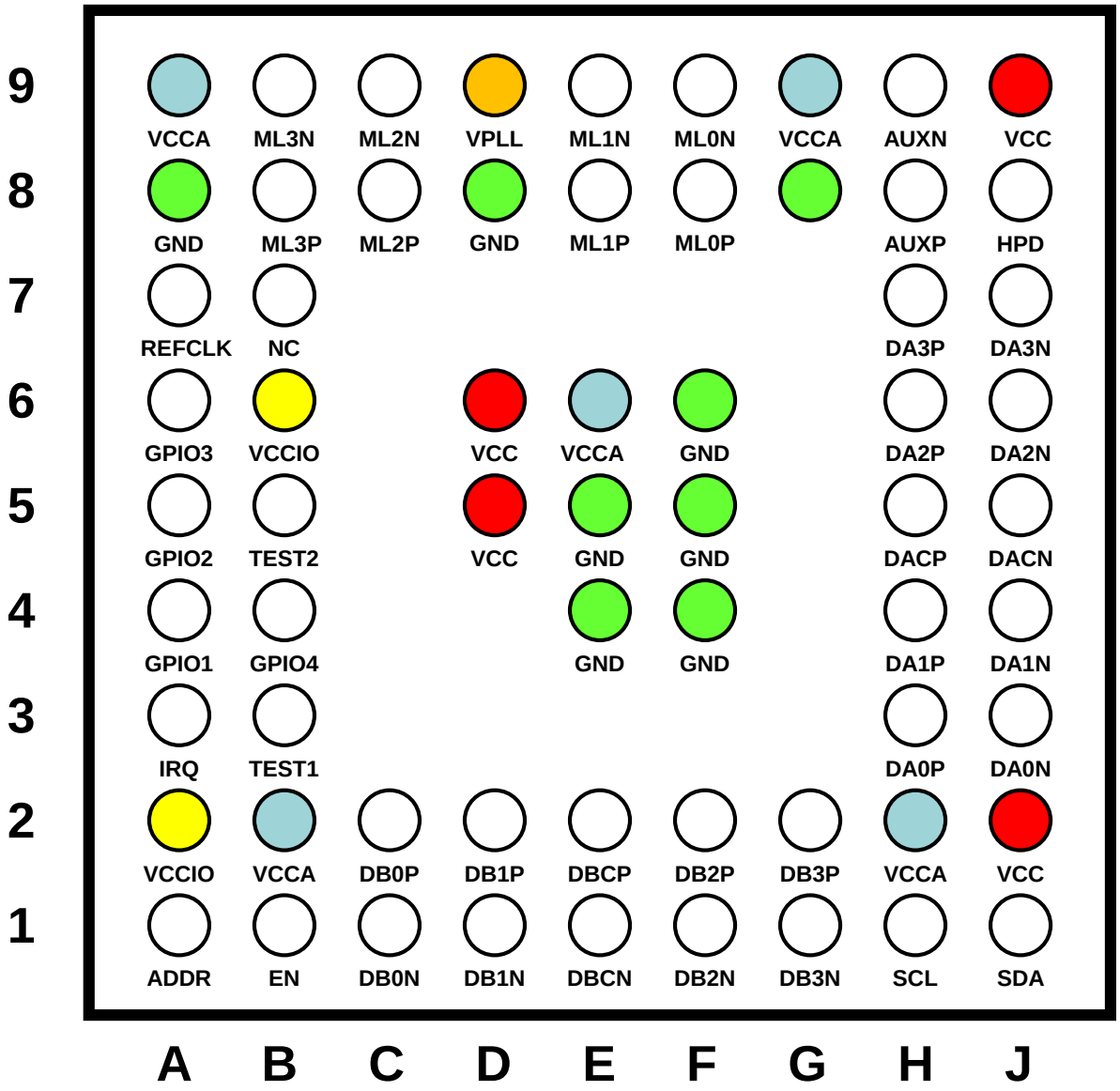



**Figure 1. Functional Block Diagram**

ZQE PACKAGE
(TOP VIEW)

# SN65DSIX6 (Top View)




To minimize the power supply noise floor, provide good decoupling near the SN65DSIX6 power pins. The use of four ceramic capacitors (2x 0.1 µF and 2x 0.1 µF) provides good performance. At the very least, it is recommended to install one 0.1 µF and one 0.01 µF capacitor near the SN65DSIX6. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized. Placing the capacitor underneath the SN65DSIX6 on the bottom of the PCB is often a good choice.

Note: The power supplies VPLL, VCCIO, VCCA, and VCC, can be applied simultaneously.

## PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| SIGNAL | NO | | |
| DA0P/N | H3, J3 | LVDS Input (HS)<br>CMOS Input/Output (LS) | MIPI® D-PHY Channel A Data Lane 0; data rate up to 1.5Gbps. |

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## PIN FUNCTIONS (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| SIGNAL | NO | | |
| DA1P/N | H4, J4 | LVDS Input (HS)<br>CMOS Input (LS)<br>(Failsafe) | MIPI® D-PHY Channel A Data Lane 1; data rate up to 1.5Gbps. |
| DA2P/N | H6, J6 | LVDS Input (HS)<br>CMOS Input (LS)<br>(Failsafe) | MIPI® D-PHY Channel A Data Lane 2; data rate up to 1.5Gbps |
| DA3P/N | H7, J7 | LVDS Input (HS)<br>CMOS Input (LS)<br>(Failsafe) | MIPI® D-PHY Channel A Data Lane 3; data rate up to 1.5Gbps. |
| DACP/N | H5, J5 | LVDS Input (HS)<br>CMOS Input (LS)<br>(Failsafe) | MIPI® D-PHY Channel A Clock Lane; operates up to 750MHz. Under proper conditions, this clock can be used instead of REFCLK to feed DisplayPort PLL. |
| DB0P/N | C2, C1 | LVDS Input (HS)<br>CMOS Input (LS)<br>(Failsafe) | MIPI® D-PHY Channel B Data Lane 0; data rate up to 1.5Gbps. |
| DB1P/N | D2, D1 | LVDS Input (HS)<br>CMOS Input (LS)<br>(Failsafe) | MIPI® D-PHY Channel B Data Lane 1; data rate up to 1.5Gbps. |
| DB2P/N | F2, F1 | LVDS Input (HS)<br>CMOS Input (LS)<br>(Failsafe) | MIPI® D-PHY Channel B Data Lane 2; data rate up to 1.5Gbps. |
| DB3P/N | G2, G1 | LVDS Input (HS)<br>CMOS Input (LS)<br>(Failsafe) | MIPI® D-PHY Channel B Data Lane 3; data rate up to 1.5Gbps. |
| DBCP/N | E2, E1 | LVDS Input (HS)<br>CMOS Input (LS)<br>(Failsafe) | MIPI® D-PHY Channel B Clock Lane; operates up to 750MHz. |
| ML0P/N | F8, F9 | LVDS output (DP) | DisplayPort Lane 0 transmit differential pair. Supports 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, and 5.4Gbps.<br>All DisplayPort lanes transmit at the same datarate. |
| ML1P/N | E8, E9 | LVDS output (DP) | DisplayPort Lane 1 transmit differential pair. Supports 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, and 5.4Gbps.<br>All DisplayPort lanes transmit at the same datarate. |
| ML2P/N | C8, C9 | LVDS output (DP) | DisplayPort Lane 2 transmit differential pair. Supports 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, and 5.4Gbps.<br>All DisplayPort lanes transmit at the same datarate. |
| ML3P/N | B8, B9 | LVDS output (DP) | DisplayPort Lane 3 transmit differential pair. Supports 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, and 5.4Gbps.<br>All DisplayPort lanes transmit at the same datarate. |
| AUXP/N | H8, H9 | LVDS I/O | Aux Channel Differential Pair. |
| TEST1 | B3 | CMOS Input<br>with internal pulldown. | Used for Texas Instruments internal use only. This pin must be left unconnected or tied to ground. |
| TEST2 | B5 | CMOS Input/Output<br>with internal pulldown | Used for internal test, HBR2 Compliance Eye, and Symbol Error Rate Measurement pattern. For normal operation this pin should be pull-down to GND or left unconnected. Refer to DP Training and Compliance Patterns for information on HBR2 Compliance Eye and Symbol Error Rate Measurement patterns. |
| EN | B1 | CMOS Input<br>(Failsafe) | Chip Enable and Reset. Device is reset (shutdown) when EN is low.<br>De-assertion (low) of EN will cause all internal CSRs and functions to be reset to default state. |
| SCL | H1 | OpenDrain Input/Output<br>(Failsafe) | Local $I^2C$ Interface Clock. . |
| SDA | J1 | OpenDrain Input/Output<br>(Failsafe) | Local $I^2C$ Interface Bi-directional Data Signal. |
| IRQ | A3 | CMOS Output | Interrupt Signal. |

## PIN FUNCTIONS (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| SIGNAL | NO | | |
| REFCLK | A7 | Input | REFCLK. Frequency determined by value programmed in I2C register or value of GPIO[3:1] latched at rising edge of EN. Supported frequencies are: 12MHz, 19.2MHz, 26MHz, 27MHz, and 38.4MHz.<br>This pin must be tied to GND when DACP/N feeds the DisplayPort PLL |
| GPIO[4:1] | B4, A6, A5, A4 | CMOS Input/Output | General Purpose I/O. Refer to GENERAL PURPOSE INPUT AND OUTPUTS for details on GPIO functionality.<br>When these pins are set high, they should be tied to the same 1.8V power rail where the SN65DSI8X VCCIO 1.8V power rail is connected. |
| HPD | J8 | CMOS Input with internal pulldown.<br>(Failsafe) | HPD input. This input requires a 51K 1% series resistor. |
| ADDR | A1 | CMOS Input/Output | Local $I^2C$ Interface Target Address Select. See Table 5. In normal operation, this pin is an input. When the ADDR pin is programmed high, it should be tied to the same 1.8 V power rails where the SN65DSI8X VCCIO 1.8 V power rail is connected. |
| NC | B7 | NA | No Connect. Leave unconnected on PCB. |
| VCCA | A9, G9, E6, B2, H2 | Power Supply | 1.2V Power Supply for Analog Circuits.<br>AVCC and VCC can be applied simultaneously. |
| VCC | D6, D5, J2, J9 | Power Supply | 1.2V Power Supply for digital core |
| VPLL | D9 | Power Supply | 1.8V Power Supply for DisplayPort PLL |
| VCCIO | B6, A2 | Power Supply | 1.8V Power Supply for Digital I/O |
| GND | A8, D8, E4, E5, F4, F5, F6, G8 | Power Supply | Reference Ground for Digital and Analog Circuits. |

## ORDERING INFORMATION(1)

| PART NUMBER | PART MARKING | PACKAGE / SHIPPING |
|---|---|---|
| SN65DSI86ZQER | DSI86 | 64-Ball PBGA / Reel |
| SN65DSI86ZQET | DSI86 | 64-Ball PBGA / Small Quantity Tape |
| SN65DSI96ZQER | DSI96 | 64-Ball PBGA / Reel |
| SN65DSI96ZQET | DSI96 | 64-Ball PBGA / Small Quantity Tape |

(1) For the most current package and ordering information, see the TI web site at www.ti.com.

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## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range | $V_{CCA}$ , $V_{CC}$ | –0.3 | 1.3 | V |
| | $V_{CCIO}$, $V_{PLL}$ | –0.3 | 2.175 | |
| Input voltage range | All input terminals | –0.5 | 2.175 | V |
| Storage temperature | $T_S$ | –65 | 105 | °C |
| Electrostatic discharge | Human Body Model (2) | | ±4 | kV |
| | Charged-device model (3) | | ±500 | V |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(3) Tested in accordance with JEDEC Standard 22, Test Method C101-A

## THERMAL INFORMATION

| | | | ZQE TYPICAL | UNIT |
|---|---|---|---|---|
| $\Theta_{JB}$ | Junction-to-board thermal resistance | | 32.9 | °C/W |
| $\Theta_{JCT}$ | Junction-to-case-top thermal resistance | | 35.7 | |
| $\psi_{JB}$ | Junction-to-board thermal resistance metric | High-K board (1) | 35.8 | |
| $\psi_{JT}$ | Junction-to-top thermal resistance metric | High-K board (1) | 1.0 | |

(1) Test conditions for $\psi_{JB}$ and $\psi_{JT}$ are clarified in TI document SPRA953A, IC Package Thermal Metrics.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | VCCA Power supply; analog circuits | 1.14 | 1.2 | 1.26 | V |
| $V_{CC}$ | VCC Power supply; digital circuits | 1.14 | 1.2 | 1.26 | V |
| $V_{CCIO}$ | VCCIO Power Supply; digital IOs. | 1.65 | 1.8 | 1.98 | V |
| $V_{PLL}$ | VPLL Power Supply, DisplayPort PLL | 1.65 | 1.8 | 1.98 | V |
| $V_{PSN}$ | Supply noise on any VCC terminal | $f_{(noise)}$ > 1MHz | | 0.05 | V |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 105 | °C |
| $T_{CASE}$ | Case temperature | | | 92.2 | °C |
| $V_{DSI\_PIN}$ | DSI input pin voltage range | –50 | | 1350 | mV |
| $f_{(I2C)}$ | Local $I^2C$ input frequency | | | 400 | kHz |
| $f_{HS\_CLK}$ | DSI HS clock input frequency | 40 | | 750 | MHz |
| $Z_L$ | DP output differential load impedance | 90 | | 110 | Ω |

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## DC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Standard IO (TEST1, TEST2, ADDR, SCL, SDA, IRQ, REFCLK, EN, GPIO[4:1])** | | | | | | |
| $V_{IL}$ | Low-level control signal input voltage | | | | 0.3 x $V_{CCIO}$ | V |
| $V_{IH}$ | High-level control signal input voltage | | 0.7 x $V_{CCIO}$ | | | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –2 mA | 1.3 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 mA | | | 0.4 | V |
| $I_{IH}$ | High level input current | Any input terminal | | | ±5 | µA |
| $I_{IL}$ | Low level input current | | | | | |
| $I_{OZ}$ | High-impedance output current | Any output terminal | | | ±10 | µA |
| $I_{OS}$ | Short-circuit output current | Any output driving GND short | | | ±2 | mA |
| $I_{CCA}$ | $V_{CCA}$ Device active current | $V_{CCA}$ = 1.2 V (2) | | 70 | 126 | mA |
| $I_{CC}$ | $V_{CC}$ Device active current | $V_{CCA}$ = 1.2 V (2) | | 43 | 52 | mA |
| $I_{CCIO}$ | $V_{CCIO}$ and $V_{PLL}$ Device Active Current | $V_{CCIO}$ = 1.8 V $V_{PLL}$ = 1.8 V (2) | | 32 | 32 | mA |
| $I_{SUSPEND\_CCA}$ | $V_{CCA}$ Device SUSPEND current | All data and clock lanes are in ultra-low power state (ULPS) and SUSPEND = 1 | | 9.8 | | mA |
| $I_{SUSPEND\_CC}$ | $V_{CC}$ Device SUSPEND current | All data and clock lanes are in ultra-low power state (ULPS) and SUSPEND = 1 | | 9 | | mA |
| $I_{SUSPEND\_CCIO}$ | $V_{CCIO}$ and $V_{PLL}$ Device SUSPEND current | All data and clock lanes are in ultra-low power state (ULPS) and SUSPEND = 1 | | 1.16 | | mA |
| $I_{EN\_CCA}$ | $V_{CCA}$ SHUTDOWN current | EN = 0 | | 0.95 | | mA |
| $I_{EN\_CC}$ | $V_{CC}$ SHUTDOWN current | EN = 0 | | 2 | | mA |
| $I_{EN\_CCIO}$ | $V_{CCIO}$ and $V_{PLL}$ SHUTDOWN current | EN = 0 | | 0.038 | | mA |
| $R_{EN}$ | EN control input resistor | | | 200 | | kΩ |
| **ADDR, EN, SCL, SDA, HPD, DBP/N[3:0], DAP/N[3:1], DBCP/N, DACP/N** | | | | | | |
| $I_{LEAK}$ | Input failsafe leakage current | $V_{CC}$ = 0; $V_{CCIO}$ = 0V. Input pulled up to $V_{CCIO}$ max. DSI inputs pulled up to 1.3V | –15 | | 15 | µA |
| **MIPI DSI INTERFACE** | | | | | | |
| $V_{IH-LP}$ | LP receiver input high threshold | See Figure 3 | 880 | | | mV |
| $V_{IL-LP}$ | LP receiver input low threshold | | | | 550 | mV |
| $V_{OH-LP}$ | LP transmitter High-level Output Voltage | | 1100 | | 1300 | mV |
| $V_{OL-LP}$ | LP transmitter Low-Level Output Voltage | | –50 | | 50 | mV |
| $\|V_{ID}\|$ | HS differential input voltage | | 70 | | 270 | mV |
| $\|V_{IDT}\|$ | HS differential input voltage threshold | | | | 50 | mV |
| $V_{IL-ULPS}$ | LP receiver input low threshold; ultra-low power state (ULPS) | | | | 300 | mV |
| $V_{CM-HS}$ | HS common mode voltage; steady-state | | 70 | | 330 | mV |
| $\Delta V_{CM-HS}$ | HS common mode peak-to-peak variation including symbol delta and interference | | | | 100 | mV |
| $V_{IH-HS}$ | HS single-ended input high voltage | See Figure 3 | | | 460 | mV |
| $V_{IL-HS}$ | HS single-ended input low voltage | | –40 | | | mV |
| $V_{TERM-EN}$ | HS termination enable; single-ended input voltage (both Dp AND Dn apply to enable) | Termination is switched simultaneous for Dn and Dp | | | 450 | mV |
| $R_{DIFF-HS}$ | HS mode differential input impedance | | 80 | | 125 | Ω |

(1) All typical values are at $V_{CC}$ = 1.2V, $V_{CCA}$ = 1.2V, $V_{CCIO}$ = 1.8V, and $V_{PLL}$ = 1.8V and $T_A$ = 25°C
(2) Maximum condition: WQXGA 60fps Dual-Link 2xDP at HBR2, PLL enabled; typical condition: WUXGA 60fps 1xDP at HBR2, PLL enabled

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## DC ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DisplayPort MAIN LINK** | | | | | | |
| $V_{TX\_DC\_CM}$ | Output common mode voltage` | | 0 | | 2 | V |
| $V_{TX\_AC\_CM\_HBR\_RBR}$ | TX AC common mode voltage for HBR and RBR. | | | | 20 | mVRMS |
| $V_{TX\_AC\_CM\_HBR2}$ | TX AC common mode voltage for HBR2 | | | | 30 | mVRMS |
| $V_{TX\_DIFFPP\_LVL0}$ | Differential peak-to-peak output voltage level 0 | Based on default state of V0_P0_VOD register | 300 | 400 | 460 | mV |
| $V_{TX\_DIFFPP\_LVL1}$ | Differential peak-to-peak output voltage level 1 | Based on default state of V1_P0_VOD register | 450 | 600 | 690 | mV |
| $V_{TX\_DIFFPP\_LVL2}$ | Differential peak-to-peak output voltage level 2 | Based on default state of V2_P0_VOD register | 600 | 800 | 920 | mV |
| $V_{TX\_DIFFPP\_LVL3}$ | Differential peak-to-peak output voltage level 3 | Based on default state of V3_P0_VOD register. Level 3 is not enabled by default. | 600 | 800 | 920 | mV |
| $V_{TX\_PRE\_RATIO\_0}$ | Pre-emphasis Level 0 | | 0 | 0 | 0 | dB |
| $V_{TX\_PRE\_RATIO\_1}$ | Pre-emphasis Level 1 | | 2.8 | 3.5 | 4.2 | dB |
| $V_{TX\_PRE\_RATIO\_2}$ | Pre-emphasis Level 2 | | 4.8 | 6.0 | 7.2 | dB |
| $V_{TX\_PRE\_RATIO\_3}$ | Pre-emphasis Level 3 | Level 3 is not enabled by default. | 4.8 | 6.0 | 7.2 | dB |
| $V_{TX\_PRE\_POST2\_RATIO\_0}$ | Post-Cursor2 Level 0 | | 0 | 0 | 0 | dB |
| $V_{TX\_PRE\_POST2\_RATIO\_1}$ | Post-Cursor2 Level 1 | | -1.1 | -0.9 | -0.7 | dB |
| $V_{TX\_PRE\_POST2\_RATIO\_2}$ | Post-Cursor2 Level 2 | | -2.3 | -1.9 | -1.5 | dB |
| $V_{TX\_PRE\_POST2\_RATIO\_3}$ | Post-Cursor2 Level 3 | Level 3 is not enabled by default. | -3.7 | -3.1 | -2.5 | dB |
| $I_{TX\_SHORT}$ | TX short circuit current limit | | | | 50 | mA |
| $R_{TX\_DIFF}$ | Differential Impedance | | 80 | 100 | 120 | Ω |
| $C_{AC\_COUPLING}$ | AC Coupling Capacitor | | 75 | | 200 | nF |
| **DisplayPort HPD** | | | | | | |
| $V_{HPD\_PLUG}$ | Hot Plug Detection Threshold | Measured at 51K series resistor. | 2.2 | | | V |
| $V_{HPD\_UNPLUG}$ | Hot Unplug Detection Threshold | Measured at 51K series resistor. | | | 0.8 | V |
| RHPDPD | HPD internal pulldown resistor | | 51 | 60 | 69 | kΩ |
| **DisplayPort AUX INTERFACE** | | | | | | |
| $V_{AUX\_DIFF\_PP\_TX}$ | Peak-to-Peak differential voltage at transmit pins | $V_{AUX\_DIFF\_PP} = 2 \times \lvert V_{AUXP} - VA_{UXN} \rvert$ | 0.18 | | 1.38 | V |
| $V_{AUX\_DIFF\_PP\_RX}$ | Peak-to-Peak differential voltage at receive pins | $V_{AUX\_DIFF\_PP} = 2 \times \lvert V_{AUXP} - V_{AUXN} \rvert$ | 0.14 | | 1.36 | V |
| $R_{AUX\_TERM}$ | AUX Channel termination DC resistance | | | 100 | | Ω |
| $V_{AUX\_DC\_CM}$ | AUX Channel DC common mode voltage | | 0 | | 1.2 | V |
| $V_{AUX\_TURN\_CM}$ | AUX Channel turnaround common-mode voltage | | | | 0.3 | V |
| $I_{AUX\_SHORT}$ | AUX Channel short circuit current limit | | | | 90 | mA |
| $C_{AUX}$ | AUX AC-coupling capacitor | | 75 | | 200 | nF |

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## SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| **MIPI DSI INTERFACE** | | | | | | |
| $t_{GS}$ | DSI LP glitch suppression pulse width | | | | 300 | ps |
| $T_{HS-SETUP}$ | DSI HS Data to Clock Setup Time | | 0.2 | | | UI |
| $T_{HS-HOLD}$ | DSI HS Clock to Data Hold Time | | 0.2 | | | UI |
| **DisplayPort MAIN LINK** | | | | | | |
| $F_{BR7}$ | Bit Rate 7 | | 5.37138 | 5.4 | 5.40162 | Gbps |
| $F_{BR6}$ | Bit Rate 6 | | 4.297104 | 4.32 | 4.321296 | Gbps |
| $F_{BR5}$ | Bit Rate 5 | | 3.222828 | 3.24 | 3.240972 | Gbps |
| $F_{BR4}$ | Bit Rate 4 | | 2.68569 | 2.7 | 2.70081 | Gbps |
| $F_{BR3}$ | Bit Rate 3 | | 2.417121 | 2.43 | 2.430729 | Gbps |
| $F_{BR2}$ | Bit Rate 2 | | 2.148552 | 2.16 | 2.160648 | Gbps |
| $F_{BR1}$ | Bit Rate 1 | | 1.611414 | 1.62 | 1.620486 | Gbps |
| $UI_{BR7}$ | Unit Interval for BR7 | High Limit = +300ppm. Low Limit = –5300ppm | | 185 | | ps |
| $UI_{BR6}$ | Unit Interval for BR6 | High Limit = +300ppm. Low Limit = –5300ppm | | 231.5 | | ps |
| $UI_{BR5}$ | Unit Interval for BR5 | High Limit = +300ppm. Low Limit = –5300ppm | | 308.6 | | ps |
| $UI_{BR4}$ | Unit Interval for BR4 | High Limit = +300ppm. Low Limit = –5300ppm | | 370.4 | | ps |
| $UI_{BR3}$ | Unit Interval for BR3 | High Limit = +300ppm. Low Limit = –5300ppm | | 411.5 | | ps |
| $UI_{BR2}$ | Unit Interval for BR2 | High Limit = +300ppm. Low Limit = –5300ppm | | 463 | | ps |
| $UI_{BR1}$ | Unit interval for BR1 | High Limit = +300ppm. Low Limit = –5300ppm | | 617.3 | | ps |
| $T_{DP\_R}$ | Differential output rise time | | 50 | | 130 | ps |
| $T_{DP\_F}$ | Differential output fall time | | 50 | | 130 | ps |
| $T_{TX\_RISE\_FALL\_MISMATCH}$ | Lane Intra-pair output skew at TX pins | | | | 5 | % |
| $T_{INTRA\_SKEW}$ | Intra-pair differential skew | | | | 20 | ps |
| $T_{INTER\_SKEW}$ | Inter-pair differential skew | | | | 100 | ps |
| $T_{TX\_EYE\_HBR2}$ | Minimum TX Eye Width at TX package pins for HBR2(2) | | 0.73 | | | $UI_{HBR2}$ |
| $T_{TX\_EYE\_MED\_TO\_MAX\_JIT\_HBR2}$ | Maximum time between the jitter median and maximum deviation from the median at TX package pins for HBR2(2) | | | | 0.135 | $UI_{HBR2}$ |
| $T_{TX\_EYE\_HBR}$ | Minimum TX Eye Width at TX package pins for HBR(2) | | 0.72 | | | $UI_{HBR}$ |
| $T_{TX\_EYE\_MED\_TO\_MAX\_JIT\_HBR}$ | Maximum time between the jitter median and maximum deviation from the median at TX package pins for HBR(2) | | | | 0.147 | $UI_{HBR}$ |
| $T_{TX\_EYE\_RBR}$ | Minimum TX Eye Width at TX package pins for RBR(2) | | 0.82 | | | $UI_{RBR}$ |
| $T_{TX\_EYE\_MED\_TO\_MAX\_JIT\_RBR}$ | Maximum time between the jitter median and maximum deviation from the median at TX package pins for RBR(2) | | | | 0.09 | $UI_{RBR}$ |

(1) All typical values are at $V_{CC}$ = 1.2 V and $T_A$ = 25°C
(2) BR refers to BR1; HBR refers to BR; HBR2 refers to BR7.

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## SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{XSSC\_AMP}$ | Link clock down-spreading | | 0% | | 0.5% | |
| $T_{SSC\_FREQ}$ | Link clock down-spreading frequency | | 30 | | 33 | kHz |
| **DisplayPort AUX INTERFACE** | | | | | | |
| $UI_{MAN}$ | Manchester transaction unit interval | | 0.4 | | 0.6 | µs |
| $t_{auxjitter\_tx}$ | Cycle-to-cycle jitter time at transmit pins | | | | 0.08 | $UI_{MAN}$ |
| $t_{auxjitter\_rx}$ | Cycle-to-cycle jitter time at receive pins | | | | 0.04 | $UI_{MAN}$ |
| **REFCLK** | | | | | | |
| $F_{REFCLK}$ | REFCLK Frequency. Supported frequencies: 12MHz, 19.2MHz, 26MHz, 27MHz 38.4MHz | | 12 | | 38.4 | MHz |
| $T_{RISEFALL}$ | REFCLK rise and fall time | 10% to 90% | 100ps | | 23 | ns |
| $T_{REFCLK}$ | REFCLK period | | 26.0417 | | 83.333 | ns |
| $T_{pj}$ | REFCLK Peak-to-Peak Phase Jitter | | | | 50 | ps |
| Duty | REFCLK Duty Cycle | | 40% | 50% | 60% | |



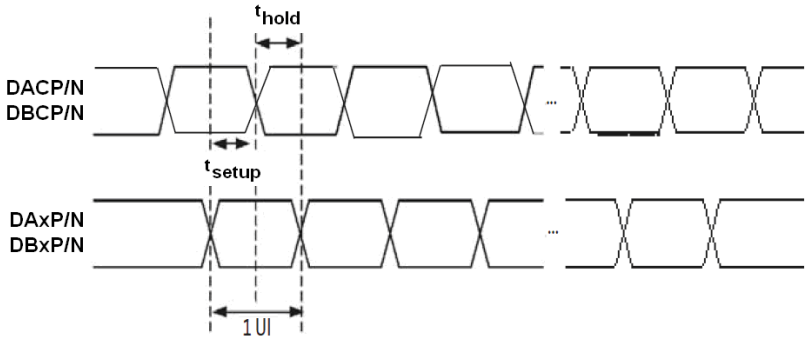


**Figure 2. DSI HS Mode Receiver Timing Definitions**

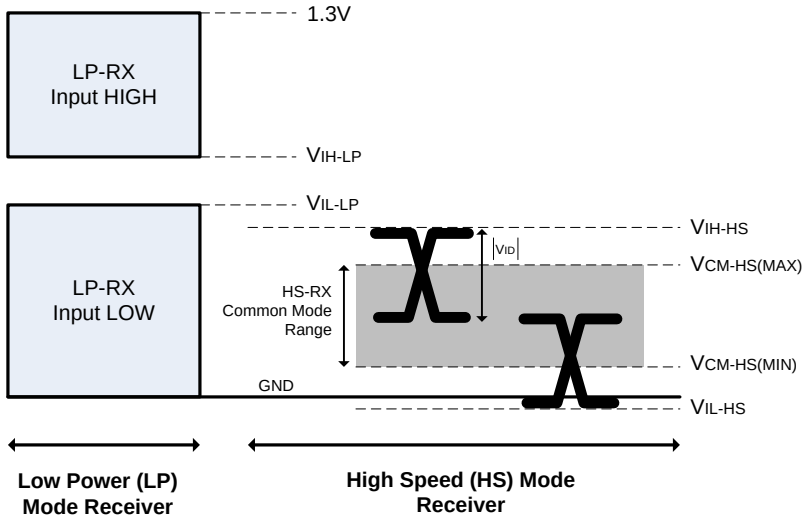


**Figure 3. DSI Receiver Voltage Definitions**

## RESET IMPLEMENTATION

When EN is de-asserted, CMOS inputs are ignored, the MIPI® D-PHY inputs are disabled, and outputs are high impedance. It is critical to transition the EN input from a low to a high level after the $V_{CC}$ supply has reached the minimum recommended operating voltage. This is achieved by a control signal to the EN input, or by an external capacitor connected between EN and GND. To insure that the SN65DSIX6 is properly reset, the EN pin must be de-asserted for at least 100 µs before being asserted.

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the VCC supply, where a slower ramp-up results in a larger value external capacitor. Refer to the latest reference schematic for the SN65DSIX6 device and/or consider approximately 200nF capacitor as a reasonable first estimate for the size of the external capacitor.

Both EN implementations are shown in the following figures.

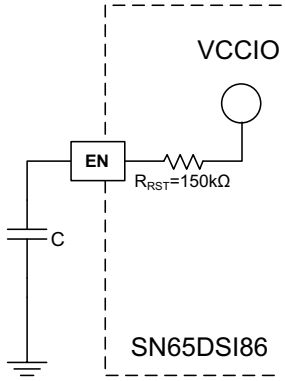


**Figure 4. External Capacitor Controlled EN**

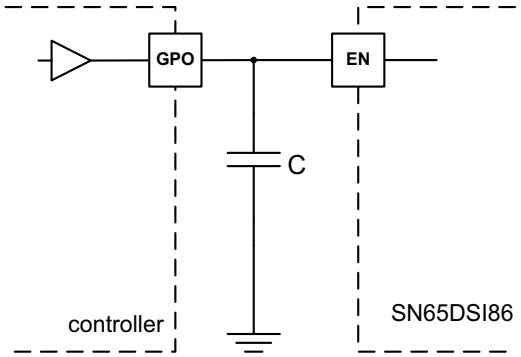


**Figure 5. EN Input from Active Controller**

### Power up Timing for DPPLL_CLK_SRC = REFCLK

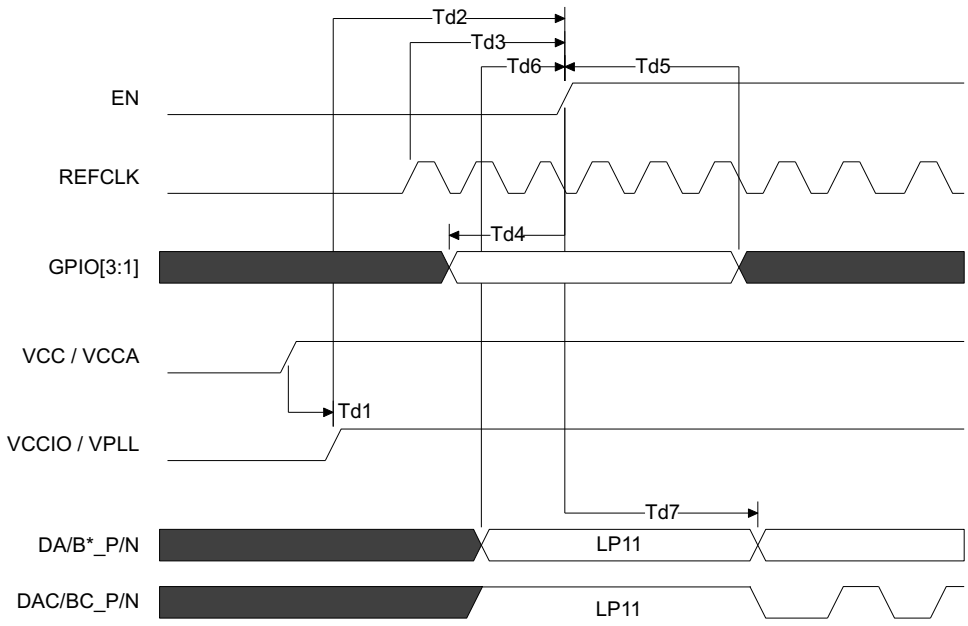


**Table 1. Power Up Requirements DPPLL_CLK_SRC = REFCLK**

| PARAMETER | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| Td1 | $V_{CC/A}$ stable before $V_{CCIO}$/$V_{PL}$L stable | 0 | |
| Td2 | $V_{CC/A}$ and $V_{CCIO}$/$V_{PLL}$ stable before EN assertion | 100 µs | |
| Td3 | REFCLK active and stable before EN assertion | 0 µs | |

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**Table 1. Power Up Requirements DPPLL_CLK_SRC = REFCLK (continued)**

| PARAMETER | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| Td4 | GPIO[3:1] stable before EN assertion | 0 ns | |
| Td5 | GPIO[3:1] stable after EN assertion | 5 µs | |
| Td6 | LP11 state on DSI channels A and B before EN assertion | 0 ns | |
| Td7 | LP11 state on DSI channels A and B after EN assertion(1) | 100 µs | |
| $T_{VCC\_RAMP}$ | $V_{CC}$ supply ramp requirements | 0.2 ms | 100 ms |
| $T_{VCCA\_RAMP}$ | $V_{CCA}$ supply ramp requirements | 0.2 ms | 100 ms |
| $T_{VCCIO\_RAMP}$ | $V_{CCIO}$ supply ramp requirements | 0.2 ms | 100 ms |
| $T_{VPLL\_RAMP}$ | $V_{PLL}$ supply ramp requirements | 0.2 ms | 100 ms |

(1) Access to DSIX6 CFR from I2C or DSI allowed after Td7.

## Power Up Timing for DPPLL_CLK_SRC = DACP/N

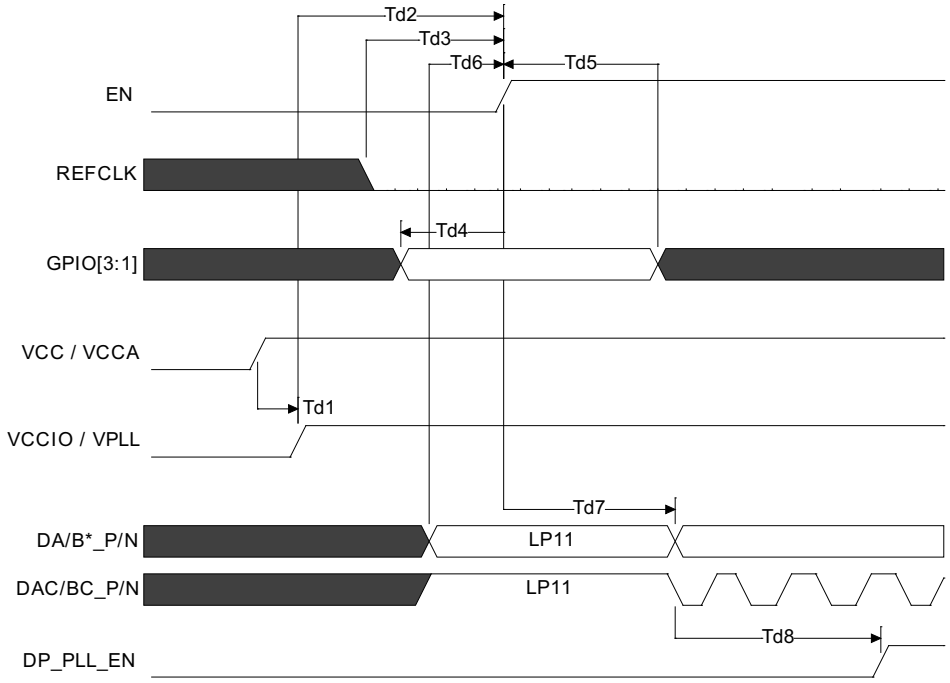


**Table 2. Power-Up Requirements for DPPLL_CLK_SRC = DACP/N**

| PARAMETER | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| Td1 | $V_{CC/A}$ stable before $V_{CCIO}$/$V_{PL}$L stable | 0 | |
| Td2 | $V_{CC/A}$ and $V_{CCIO}$/$V_{PLL}$ stable before EN assertion | 100 µs | |
| Td3 | REFCLK low before EN assertion | 10 µs | |
| Td4 | GPIO[3:1] stable before EN assertion | 0 ns | |
| Td5 | GPIO[3:1] stable after EN assertion | 5 µs | |
| Td6 | LP11 state on DSI channels A and B before EN assertion | 0 ns | |
| Td7 | LP11 state on DSI channels A and B after EN assertion(1) | 100 µs | |
| Td8 | DACP/N active and stable before DP_PLL_EN bit is set. | 100 µs | |
| $T_{VCC\_RAMP}$ | $V_{CC}$ supply ramp requirements | 0.2 ms | 100 ms |
| $T_{VCCA\_RAMP}$ | $V_{CCA}$ supply ramp requirements | 0.2 ms | 100 ms |
| $T_{VCCIO\_RAMP}$ | $V_{CCIO}$ supply ramp requirements | 0.2 ms | 100 ms |
| $T_{VPLL\_RAMP}$ | $V_{PLL}$ supply ramp requirements | 0.2 ms | 100 ms |

(1) Access to DSIX6 CFR from I2C or DSI allowed after Td7.

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## PowerUp Sequence

| STEP# | DESCRIPTION |
|---|---|
| 1. | EN de-asserted (LOW) and all Power Supplies active and stable. Depending on whether DPPLL_CLK_SRC is REFCLK pin or the DACP/N pins, GPIO[3:1] set to value that matches the REFCLK or DACP/N frequency. Refer to Table 10 for GPIO to REFCLK/DACP/N frequency combinations. If GPIO are not going to be used to select the REFCLK/DACP/N frequency, then software must program the REFCLK_FREQ register via I2C after the EN is asserted. This knowledge of the REFCLK_FREQ is also used by the DSIX6 to determine the DSI Clock frequency when DPPLL_CLK_SRC is REFCLK pin. |
| 2. | EN is asserted (HIGH). |
| 3 | Configure number of DSI channels and lanes per channel. The DSIX6 defaults to 1 lane of DSI Channel A. DSI Channel B is disabled by default. When using DSI to configure the DSIX6, software need to keep in mind the default configuration of the DSI channels only allows access to internal CSR through either 1 lane of HSDT or LPDT. Once CFR defaults are changed, all future CFR accesses should use the new DSI configuration. DSI Channel B can never be used to access internal DSI8X CSR space. $I^2C$ access to internal DSIX6's CSR is always available. |
| 4. | Configure REFCLK or DACP/N Frequency. If GPIO[3:1] is used to set the REFCLK or DACP/N frequency, then this step can be skipped. This step must be completed before any DisplayPort AUX channel communication can occur. SW needs to program REFCLK_FREQ to match the frequency of the clock provided to REFCLK pin or DACP/N pins. The knowledge of the REFCLK_FREQ is also used by the DSIX6 to determine the DSI Clock frequency when DPPLL_CLK_SRC is REFCLK pin. |
| 5 | The DSIX6 supports polarity inversion of each of the MLP[3:0] and MLN[3:0] pins. The purpose of this feature is to help prevent any DisplayPort Main Link differential pair crossing on the PCB. If the system implementer uses this feature, then the MLx_POLR registers need to be updated to match the system implementation. |
| 6 | The DSIX6 supports the ability to assign physical MLP/N[3:0] pins to a specific logical lane in order to help in the routing on the PCB. By default, physical pins MLP/N0 is logical lane 0, physical pins MLP/N1 is logical lane 1, physical pins MLP/N2 is logical lane 2, and physical pins MLP/N3 is logical lane 3. If the actual system implementation does not match the DSIX6 default values, then the LNx_ASSIGN fields need to be updated to match the system implementation. |
| 7 | By default, all interrupt sources are disabled (IRQ will not get asserted). SW needs to enable interrupt sources it cares about. |
| 8 | In an eDP application, HPD is not required. If HPD is not used, software needs to disable HPD by writing to the HPD_DISABLE register and then go to the next step. If HPD is used, then software shall remain in this step until an HPD_INSERTION occurs. Once a HPD_INSERTION occurs, software can go to the next step. |
| 9. | Resolution capability of eDP Panel through reading EDID. In a eDP application, the Panel resolution capability may be known in advance. If this is the case, then this step can be skipped. Two methods are available for reading the EDID: direct method and indirect method. |
| | 1. Using the direct method, SW needs to program I2C_ADDR_CLAIMx registers and enable them. Once this is done, any $I^2C$ transaction that targets the I2C_ADDR_CLAIMx address will be translated into a I2C-Over-AUX transaction. In order to use the direct method, the I2C master must support clock stretching. |
| | 2. Using the indirect method, SW needs to use Native and I2C-Over-Aux registers. When using the indirect method, the max read size allowed is 16-bytes. This means reading the EDID must be broken into 16-byte chunks. |
| 10. | eDP Panel DisplayPort Configuration Data (DPCD). In a eDP applications, the eDP panel DPCD information maybe known in advance. If this is the case, then this step can be skipped. SW can obtain the DPCD information by using the Native Aux Registers. The eDP panel capability is located at DisplayPort Address 0x00000 thru 0x0008F. When reading the DPCD capability, sw needs to be aware that Native Aux transactions, like I2C-Over-Aux, is limited to a read size of 16-bytes. This means SW must read the DPCD in 16-byte chunks. |
| 11. | Based on resolution and capabilities of eDP sink obtain from EDID and DPCD, GPU should program the appropriate number of data lanes (DP_NUM_LANES) and datarate (DP_DATARATE) to match source capabilities and sink requirements. SSC_ENABLE can also be set if the eDP sink supports SSC. |
| 12. | Enable the DisplayPort PLL by writing a '1' to the DP_PLL_EN register. Before proceeding to next step, software should verify the PLL is locked by reading the DP_PLL_LOCK bit. |
| 13. | The SN65DSIX6 only supports ASSR Display Authentication method and this method is enabled by default . An eDP panel must support this Authentication method. Software will need to enable this method in the eDP panel at DisplayPort address 0x0010A. |
| 14. | Train the DisplayPort Link. Based on the resolution requirements of the application and the capabilities of the eDP panel, software needs to choose the optimum lane count and datarate for DisplayPort Main Links. The DSIX6 provides three methods for Link Training: Manual, Fast, and Semi-Auto. |
| | 1. Manual Method is completely under SW control. SW can follow training steps outlined in the DisplayPort Standard or sw can perform a subset of what the DisplayPort standard requires. |
| | 2. Fast Link Train. Prior knowledge of the calibrated settings is required in order to use Fast Link Train. SW needs to program both the DSIX6 and the eDP panel with the calibrated settings. Once this is done, software can change the ML_TX_MODE from Main Link Off to Fast Link Training. The DSIX6 will transmit the enabled TPS1 and/or TPS2 pattern and then transition the ML_TX_MODE to Normal Mode. |

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| STEP# | DESCRIPTION |
|---|---|
| | 3. Semi-Auto Link Training. This method is intended if there is a preferred datarate and lane count but the other parameters like TX_SWING and Pre-Emphasis are not known or eDP sink does not support Fast Training. SW can transition the ML_TX_MODE to Semi-Auto Link Training. If training is successful, the LT_PASS flag will get set and the ML_TX_MODE will be transitioned to Normal Mode. If training is unsuccessful, the LT_FAIL flag will get set and the ML_TX_MODE will transition to Main Link Off. SW then will have to specify a different data rate and/or lane count combination and attempt Auto-Link training again. This is repeated until successful link training occurs. Please keep in mind that changes in data rate will cause the DP PLL to lose lock. SW should always wait until DP_PLL_LOCK bit is set before attempting another Semi-Auto Link training. |
| 15. | Video Registers need to be programmed. Video Registers are used by the DSIX6 to recreate the video timing provided from the DSI interface to the DisplayPort interface. |
| 16. | Configure GPIO control registers if default state if not used. The GPIO default to Inputs. |
| 17. | Configure *Assertive Display Core*. (For SN65DSI96 only) |
| 18. | Video stream can be enabled in the GPU and sent via the DSI interface to the DSIX6. |
| 19. | SW can now enable the DSIX6 to pass the video stream provided on the DSI interface to the DisplayPort interface by writing a '1' to the VSTREAM_ENABLE register. |

### Power Down Sequence

| STEP# | DESCRIPTION |
|---|---|
| 1. | Clear VSTREAM_ENABLE bit. |
| 2. | Stop DSI stream from GPU. DSI lanes shall be placed in LP11 state. |
| 3. | Program the ML_TX_MODE to 0x0 (OFF). |
| 4. | Program the DP_NUM_LANES register to 0x0. |
| 5. | Clear the DP_PLL_EN bit. |
| 6 | For SN65DSI96, disable Assertive Display core by clearing the ADEN bit. |
| 7. | De-assert the EN pin. |
| 8 | Remove power from supply pins ($V_{CC}$, $V_{CCA}$, $V_{CCIO}$, $V_{PLL}$) |

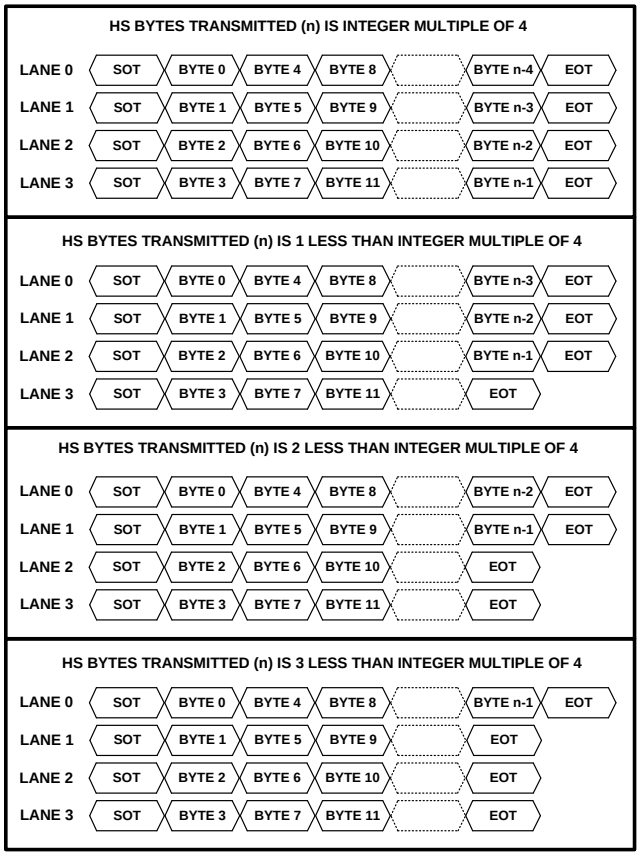


## DISPLAY SERIAL INTERFACE (DSI)

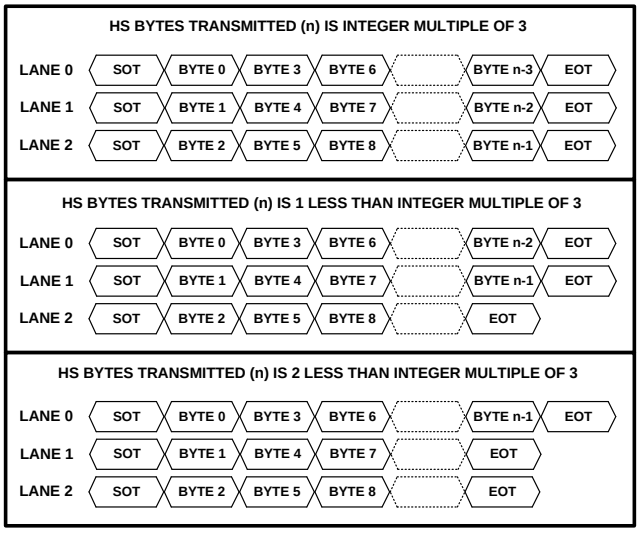
The DSI interface can be used for two purposes: (1) Configuring DSIX6 CSR. (2). Streaming RGB video to an external DisplayPort sink. When used to configure the DSIX6, all communication from the DSIX6 to the GPU (read responses) will use DSI channel A lane 0 in LP signaling mode. The DSIX6 supports communication from GPU to DSIX6 in both HS mode and LP mode.

### DSI Lane Merging

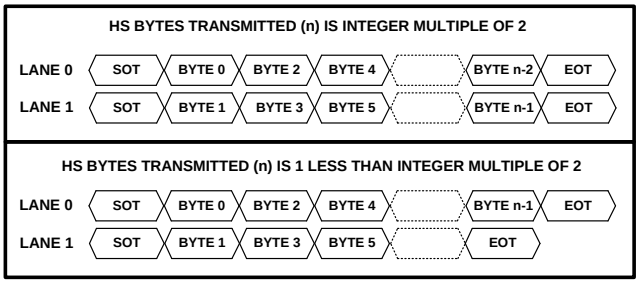
The SN65DSIX6 supports one DSI data lane per input channel by default, and may be configured to support two, three, or four DSI data lanes per channel. The bytes received from the data lanes are merged in HS mode to form packets that carry the video stream or target DSIX6 CFR space. DSI data lanes are bit and byte aligned. Figure 6 illustrates the lane merging function for each channel; 4-Lane, 3-Lane, and 2-Lane modes are illustrated.




*4 DSI Data Lane Configuration*




*3 DSI Data Lane Configuration*




*2 DSI Data Lane Configuration*

**Figure 6. SN65DSIX6 DSI Lane Merging Illustration**

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## DSI Supported Data Types

The table below summarizes the DSI data types supported by the DSIX6. Any Data Type received by the DSIX6 that is not listed below will be ignored.

**Table 3. Supported HS DSI Data Types from GPU**

| DATA TYPE | DESCRIPTION | DSI CHANNEL | PURPOSE |
|---|---|---|---|
| 0x01 | Vsync Start | A and B | Events for Video Timing |
| 0x11 | Vsync End | A and B | |
| 0x21 | Hsync Start | A and B | |
| 0x31 | HSync End | A and B | |
| 0x08 | End of Transmission packet (EoTp) | A and B | Marks the end of a HS transmission. |
| 0x09 | Null Packet | A and B | |
| 0x19 | Blanking Packet | A and B | |
| 0x24 | Generic Read Request 2 parameters | A-only | Read CFR Request |
| 0x37 | Set Maximum Return Packet Size | A-only | Specifics the maximum amount data returned from a Generic Read Request supported by GPU. |
| 0x23 | Generic Short Write 2 parameters | A-only | Configure CFR |
| 0x29 | Generic Long Write | A-only | Configure CFR and Secondary Data Packets |

**Table 3. Supported HS DSI Data Types from GPU (continued)**

| DATA TYPE | DESCRIPTION | DSI CHANNEL | PURPOSE |
|---|---|---|---|
| 0x1E | Pixel Stream 18-bit RGB-666 Packed format | A and B | Active Pixel Data |
| 0x2E | Pixel Stream 18-bit RGB-666 Loosely Packed Format | A and B | |
| 0x3E | Pixel Stream 24-bit RGB-888 format | A and B | |

**Table 4. SN65DSIX6 LPDT DSI Data Type from GPU**

| DATA TYPE | DESCRIPTION | DSI CHANNEL | PURPOSE |
|---|---|---|---|
| 0x24 | Generic Read Request 2 parameters | CHA Lane 0 | Read CFR requests |
| 0x23 | Generic Short Write 2 parameters | CHA Lane 0 | Configure CFR. |
| 0x08 | EoTp | CHA Lane 0 | Indicates end of HS transmission. |

**Table 5. SN65DSIX6 DSI Data Type Responses**

| DATA TYPE | DESCRIPTION | DSI CHANNEL | PURPOSE |
|---|---|---|---|
| 0x11 | Generic Short Read Response 1 Byte | CHA Lane 0 | LPDT Response from Read Request |
| 0x02 | Acknowledge and Error Report | CHA Lane 0 | LPDT Response following a Generic Read/Write with errors. Or an unsolicited BTA. |
| N/A | Acknowledge Trigger Message | CHA Lane 0 | Trigger Message used to indicate no errors detected in Generic Request. |



## Generic Request Datatypes

The Generic Request datatypes are used for reading and writing to DSIX6's CFR space as well as for providing DisplayPort's secondary data packets. The DSIX6 supports these request types in the form of high-speed data transmissions or low power data transmissions (LPDT).

In order to properly sample high speed data received on the DSI interface, the DSIX6 implements a hardware mechanism, known as DSI_CLK_RANGE Estimator, to determine the DSI clock frequency. This hardware mechanism uses the REFCLK as a reference for calculating the DSI clock frequency. When the REFCLK_FREQ register correctly matching the REFCLK frequency, the DSI_CLK_RANGE Estimator will be able determine the DSIA and DSIB clock frequency. The DSI_CLK_RANGE Estimator requires a throw-away read (i.e. read from address 0x00) before hardware will update CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE registers. Note that this first access may set some DSI error bits. In the cases where the system designer does not wish to use the DSI_CLK_RANGE Estimator, software can write the desired DSI Clock frequency to the CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE. Once these registers are written, the DSI_CLK_RANGE Estimator will be disabled and it becomes system software responsibility to make sure the CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE registers always reflect the actual DSI clock frequency.

### Generic Read Request 2-Parameters Request

The Generic Read Request with 2 parameters will be used for reading DSIX6's CFR registers. The current address space requirement for the DSIX6 is just 256 bytes. This means the MS Byte of ADDR (bits 15 to 8) will always be zero. The MS Byte of the ADDR is intended for future expansion. The SN65DSIX6's response size defaults to one byte as defined by [DSI]. Software can use the Set Maximum Return Packet Size to inform the DSI86 that the GPU can support more than one byte, but the DSIX6 will always provide a response of one byte. If a single-bit ECC error was detected and corrected in the request, the DSIX6 will provide the requested data along with an Acknowledge and Error Report packet. If multi-bit ECC errors are detected and not corrected, the DSIX6 will only respond with an Acknowledge and Error Report packet.

| SOT | ID = 0x24 | ADDR (LS Byte) | ADDR (MS Byte) | ECC | EOT |
|---|---|---|---|---|---|

**Figure 7. Generic Read Request 2 Parameters Format**

### Generic Short Write 2-Parameters Request

The Generic Short Write with 2 parameters can be used for writing to DSIX6's CFR registers. The first parameter is the CFR Address and the second parameter is the data to be written to the address pointed to by the first parameter.

| SOT | ID = 0x23 | ADDR (Byte) | DATA | ECC | EOT |
|---|---|---|---|---|---|

**Figure 8. Generic Short Write Request 2 Parameters Format**

**NOTE**

If GPU completes transmission with a BTA, the DSIX6 will respond with either an Acknowledge, if no errors were detected in current or previous packets, or an Acknowledge and Error Report packet, if errors were detected in current or previous packets.

### Generic Long Write Packet Request

The Generic Long Write packet is used to write to CFRS within the DSIX6 as well as send secondary data packet to the eDP panel. The MS Byte of ADDR (bits 15 to 8) shall be used to select whether the packet is SDP or whether it targets DSIX6's CFR registers.. If the MS Byte of ADDR is equal to 0x80, then the DSIX6 will interpret the Generic Long Write to be a secondary data packet. If the MS Byte of ADDR is equal to 0x00, then the DSIX6 will interpret the Generic Long Write to target CFR space. For all other values of MS Byte of the ADDR, the DSIX6 will ignore the request and set the appropriate error flag.

| SOT | ID = 0x29 | WC (LS Byte) | WC (MS Byte) | ECC | ADDR (LS Byte) | ADDR (MS Byte) | DATA0 | DATA1 | DATA [WC-3] | CHKSUM (LS Byte) | CHKSUM (MS Byte) | EOT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

**Figure 9. Generic Long Write Format**

**NOTE**

The WC field value must include the two ADDR bytes and the amount of data to be written. For example, if the amount of data to be written is 1 byte, then the WC(LS Byte) must be 0x03 and the WC(MS Byte) must be 0x00. Also, the maximum WC field value supported by the SN65DSIX6 is 258 bytes or (0x0102). When writing to DSIX6's CFR space, the maximum WC field value supported is three bytes. If GPU completes transmission with a BTA, the DSIX6 shall respond with either an Acknowledge, if no errors were detected in current or previous packets, or an Acknowledge and Error Report packet, if errors were detected in current or previous packets.

## DSI Pixel Stream Packets

The SN65DSIX6 processes 18bpp (RGB666) and 24bpp (RGB888) DSI packets on each channel as illustrated below:

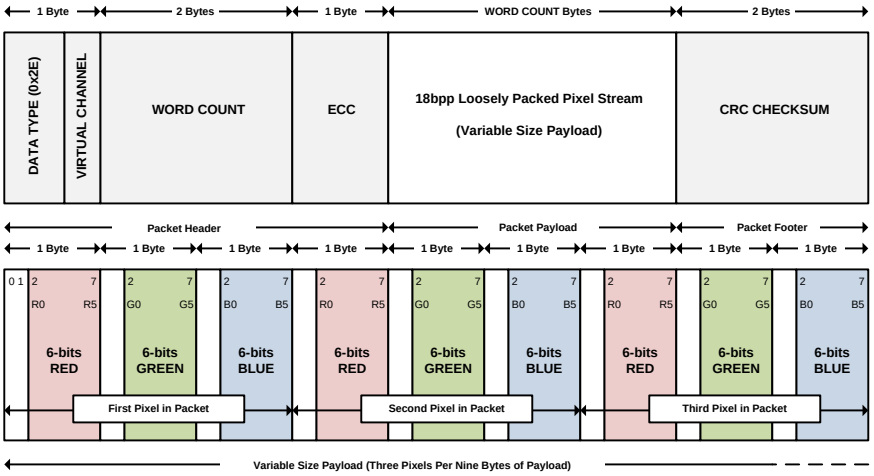


**Figure 10. 18 bpp (Loosely Packed) DSI Packet Structure**

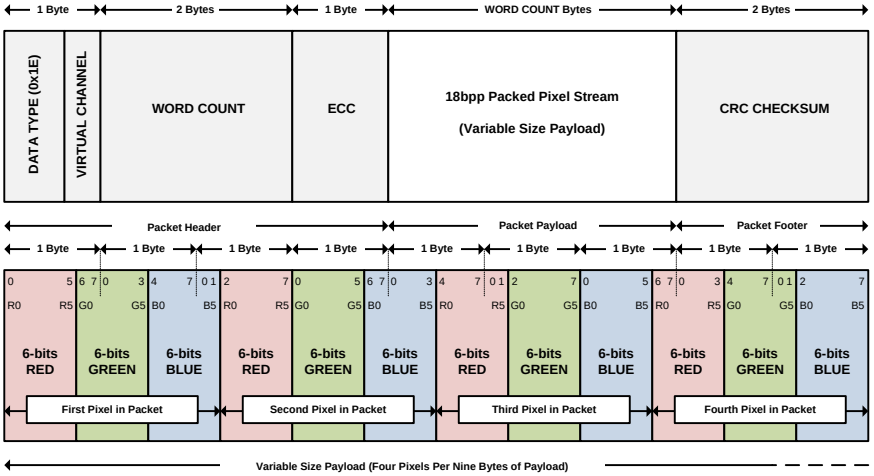


**Figure 11. 18bpp (Tightly Packed) DSI Packet Structure**

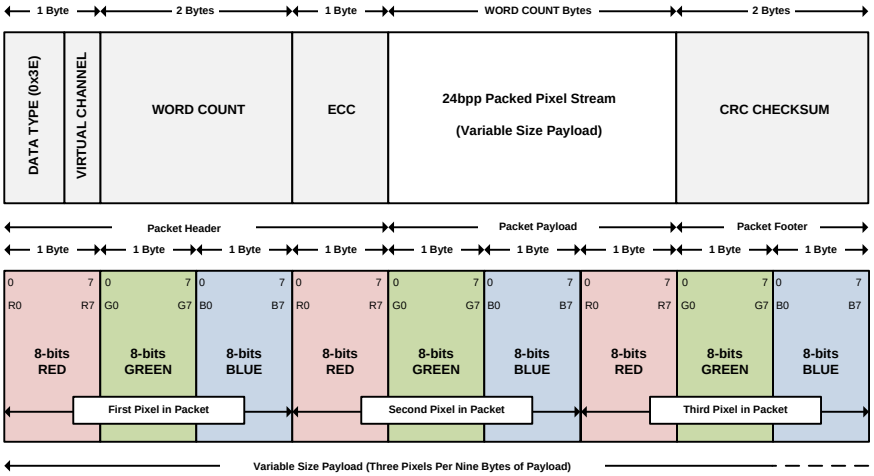


**Figure 12. 24bpp DSI Packet Structure**

**Table 6. Example of 4-Lane DSI Packet Data for 24bpp RGB**

| Lane 0 | Lane 1 | Lane 2 | Lane 3 |
|---|---|---|---|
| SOT | SOT | SOT | SOT |
| 0x3E | WC (LS Byte) | WC(MS Byte) | ECC |
| R0-7:0 | G0-7:0 | B0-7:0 | R1-7:0 |
| G1-7:0 | B1-7:0 | R2-7:0 | G2-7:0 |
| B2-7:0 | R3-7:0 | G3-7:0 | B3-7:0 |
| R4-7:0 | G4-7:0 | B4-7:0 | R5-7:0 |
| G5-7:0 | B5-7:0 | CRC (LS Byte) | CRC (MS Byte) |
| EOT | EOT | EOT | EOT |

## DSI Video Transmission Specifications

The SN65DSIX6 expects the GPU to provide video timing events and active pixel data in the proper order in the form of a real-time pixel stream. According to the DSI specification [DSI], active pixel data is transmitted in one of two modes: Non-Burst and Burst. The SN65DSIX6 supports both non-burst and burst mode packet transmission. The burst mode supports time-compressed pixel stream packets that leave added time per scan line for power savings LP mode. For a robust and low-power implementation, the transition to LP mode is recommended on every video line, although once per frame is considered acceptable.

According to the DSI specification [DSI], timing events can be provided in one of two types: Sync Pulses, and Sync Events. The SN65DSIX6 supports both types. For the Sync Pulse type of timing event, the GPU will send VSYNC START (VSS), VSYNC END (VSE), HSYNC START (HSS), and HSYNC END (HSE) packets. For Sync Event type, the GPU will only send the sync start packets (VSS and HSS). For both types of timing events, the DSIX6 will use the values programmed into the Video Registers to determine the sync end events (VSE and HSE). Please note when configured for dual DSI channels, the SN65DSIX6 will use VSS, VSE, and HSS packets from channel A. The DSIX6 will use channel A events to recreate the same timings on the DisplayPort interface. The VSS, VSE, and HSS packets from channel B are used to internally align data on channel B to channel A.

The first line of a video frame shall start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

As required in the DSI specification, the SN65DSIX6 requires that pixel stream packets contain an integer number of pixels (i.e. end on a pixel boundary); it is recommended to transmit an entire scan line on one pixel stream packet. When a scan line is broken in to multiple packets, inter-packet latency shall be considered such that the video pipeline (ie. pixel queue or partial line buffer) does not run empty (i.e. under-run); during scan line processing. If the pixel queue runs empty, the SN65DSIX6 transmits zero data (18'b0 or 24'b0) on the DisplayPort interface.

When configured for dual DSI channels, the SN65DSIX6 supports ODD/EVEN configurations and LEFT/RIGHT configurations. In the ODD/EVEN configuration, the odd pixels for each scan line are received on channel A, and the even pixels are received on channel B. In LEFT/RIGHT mode, the LEFT portion of the line is received on channel A, and the right portion of the line is received on channel B. The pixels received on channel B in LEFT/RIGHT mode are buffered during the LEFT side transmission to DisplayPort, and begin transmission to DisplayPort when the LEFT-side input buffer runs empty. The only requirement for LEFT/RIGHT mode is CHB_ACTIVE_LINE_LENGTH must be at least 1 pixel.

**NOTE**

The DSIX6 does not support the DSI Virtual Channel capability.

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**Table 7. Summary of DSI Video Input Requirements**

| NUMBER | REQUIREMENT |
|---|---|
| 1 | DSI datatypes VSS and HSS are required, but datatypes HSE and VSE are optional. |
| 2 | The exact time interval between each HSS shall be maintained. |
| 3 | The time between the HSS and HACT (known as HBP) does not have to be maintained. The DSIX6 will recreate HBP on DisplayPort. |
| 4 | The time from the end of HACT to HSS (known as HFP) does not have to be maintained. The DSIX6 will recreate HFP on DisplayPort. |
| 5 | The time from VSS to first line of active video shall be maintained. |
| 6 | The time from end of last line of active video to the beginning of the first line of active video shall be maintained. This time is defined as the Vertical Blanking period. |

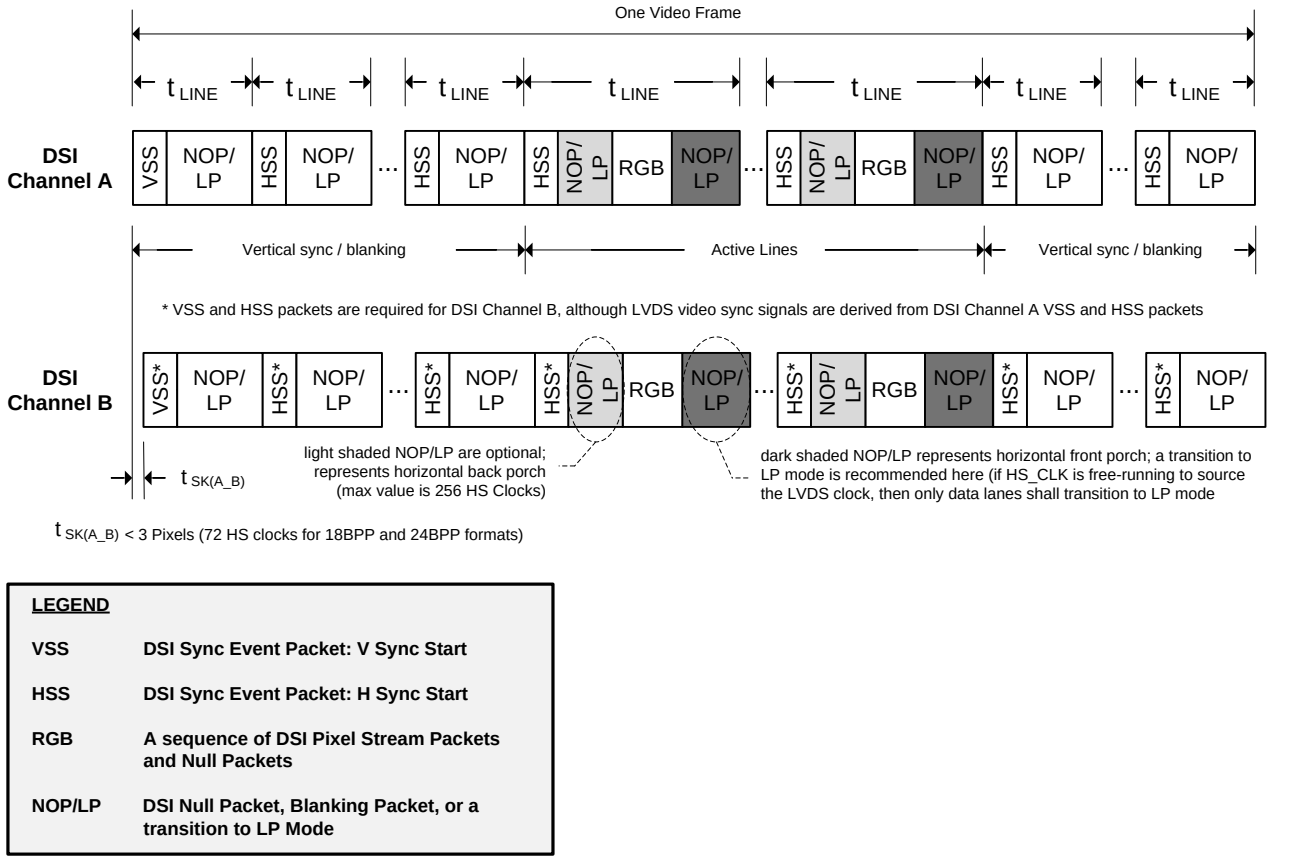


**Figure 13. DSI Channel Transmission and Transfer Function**

## Video Format Parameters

It is the responsibility of the GPU software to program the DSIX6's *Video Registers* with the Video format that is expected to be displayed on the eDP panel. The DSIX6 expects the parameters in the Table 8 to be programmed. The DSIX6 will use these parameters to determine the DisplayPort MSA parameters that are transmitted over DisplayPort every vertical blanking period. These MSA parameters are used by the eDP panel to recreate the video format provided on the DSI interface.

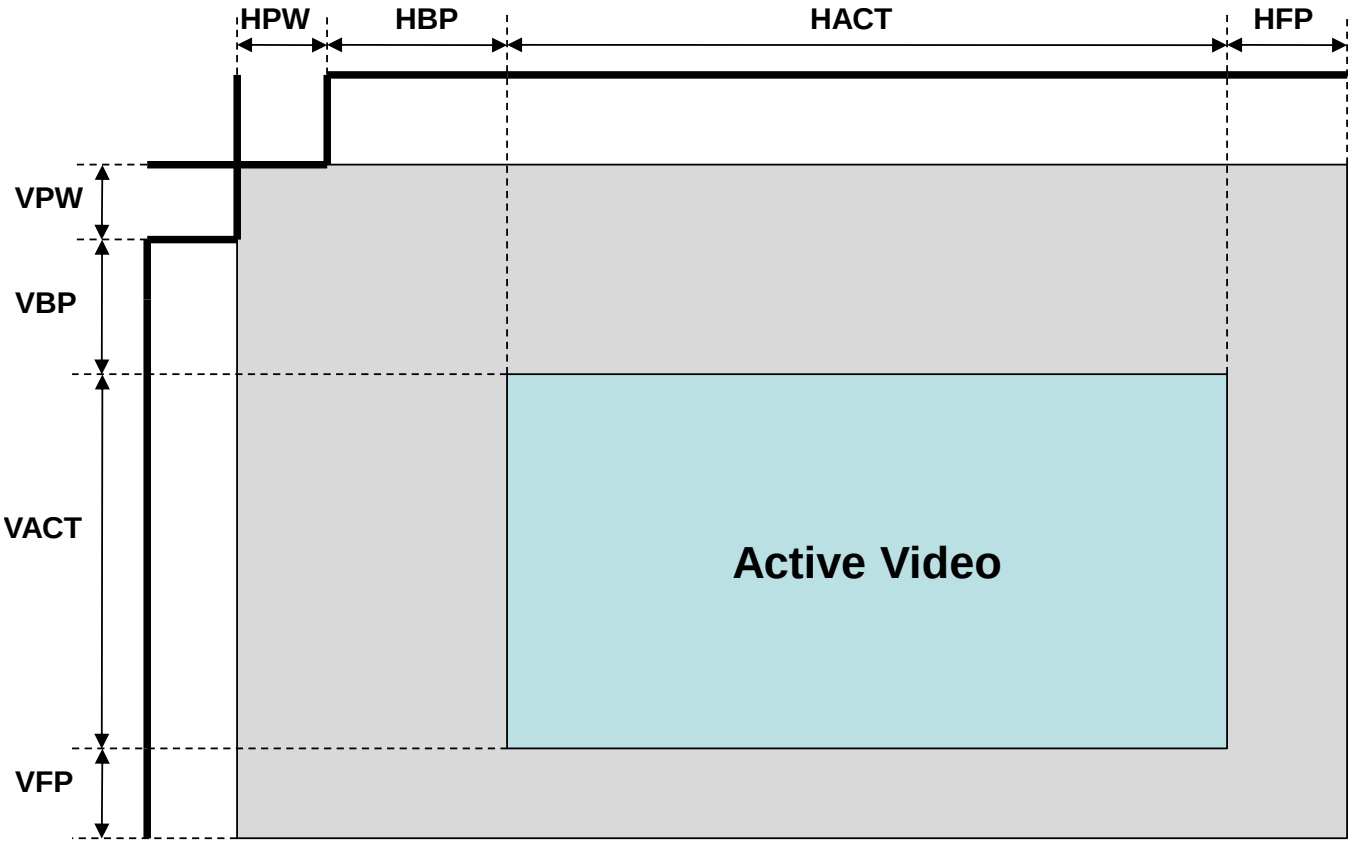


**Figure 14. Video Format**

**Table 8. Video Format Parameters**

| PARAMETER | DESCRIPTION | DSIX6 REGISTER |
|---|---|---|
| HPOL | Used to specify if the HPW is high or low. | CHA_HSYNC_POLARITY |
| HPW | The width of the Horizontal Sync Pulse in pixels | {CHA_HSYNC_PULSE_WIDTH_HIGH, CHA_HSYNC_PULSE_WIDTH_LOW} |
| HBP | The size of the Horizontal Back Porch in pixels | CHA_HORIZONTAL_BACK_PORCH |
| HACT | The length, in pixels, of the active horizontal line. | {CHA_ACTIVE_LINE_LENGTH_HIGH, CHA_ACTIVE_LINE_LENGTH_LOW} + {CHB_ACTIVE_LINE_LENGTH_HIGH, CHB_ACTIVE LINE_LENGTH_LOW} |
| HFP | The size of the Horizontal Front Porch in pixels. | CHA_HORIZONTAL_FRONT_PORCH |
| HTOTAL | Total length, in pixels, of a horizontal line. | HPW + HBP + HACT + HFP |
| VPOL | Used to specify if the VPW is high or low | CHA_VSYNC_POLARITY |
| VPW | The width of the Vertical Sync Pulse in lines. The width must be at least 1 line. | {CHA_VSYNC_PULSE_WIDTH_HIGH, CHA_VSYNC_PULSE_WIDTH_LOW} |
| VBP | The size of the Vertical Back Porch in lines. The size must be at least 1 line. | CHA_VERTICAL_BACK_PORCH |
| VACT | The number of vertical active lines. | {CHA_VERTICAL_DISPLAY_SIZE_HIGH, CHA_VERTICAL_DISPLAY_SIZE_LOW} |
| VFP | The size of the Vertical Front Porch in lines. The size must be at least 1 line. | CHA_VERTICAL_FRONT_PORCH |
| VTOTAL | The total number of vertical lines in a frame. | VPW + VBP + VACT + VFP |

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### GPU LP-TX Clock Requirements

The GPU is responsible for controlling its own LP clock frequency to match the DSIX6. The GPU LP TX clock frequency shall be in the range of 67% to 150% of the DSIX6 LP TX clock frequency. The DSIX6 LP TX clock frequency is detailed in Table 9.

**Table 9. DSIX6 LP TX Clock Frequency**

| REFCLK_FREQ | LP TX Clock Frequency |
|---|---|
| 0x0 | 12 MHz |
| 0x1 | 19.2 MHz |
| 0x2 | 13 MHz |
| 0x3 | 13.5 MHz |
| 0x4 | 19.2 MHz |

## GENERAL PURPOSE INPUT AND OUTPUTS

The DSIX6 provides four GPIO pins which can be configured as an input or output. The GPIOs default to input but can be changed to output by changing the appropriate GPIO Register.

GPIO Functions:

1. Input
2. Output
3. SUSPEND Input (powers down entire chip except for I2C interface)
4. PWM
5. DSIA VSYNC
6. DSIA HSYNC

### GPIO REFCLK and DSIA Clock Selection

The clock source for the DSIX6 is derived from one of two sources: REFCLK pin or DACP/N pins. On the rising edge of EN, the sampled state of GPIO[3:1] as well as the detection of a clock on REFCLK pin is used to determine the clock source and the frequency of that clock. After the EN, software through the $I^2C$ interface can change the configuration of REFCLK_FREQ, and CHA_DSI_CLK_RANGE for the case where GPIO[3:1] sampled state does not represent the intended functionality. Because the clock source is determined at the assertion of EN, software can not change the clock source.

**Table 10. GPIO REFCLK or DACP/N FREQUENCY SELECTION(1)(2)(3)**

| GPIO[3:1] | REFCLK FREQUENCY (DPPLL_CLK_SRC = 0) | DACP/N CLOCK FREQUENCY (DPPLL_CLK_SRC = 1) | REFCLK_FREQ |
|---|---|---|---|
| 3'b000 | 12 MHz | 468MHz (DSIACLK / 39 = 12 MHz ) | 0x0 |
| 3'b001 | 19.2 MHz | 384MHz (DSIACLK / 20 = 19.2 MHz) | 0x1 |
| 3'b010 | 26 MHz | 416MHz (DSIACLK / 16 = 26 MHz) | 0x2 |
| 3'b011 | 27 MHz | 486MHz (DSIACLK / 18 = 27 MHz) | 0x3 |
| 3'b100 | 38.4 MHz. | 460.8MHz (DSIACLK / 12 = 38.4 MHz) | 0x4 |
| 3'b101 thru 3'b111 | 19.2 MHz | 384MHz (DSIACLK / 20 = 19.2 MHz) | 0x5 thru 0x7 |

(1) For case when DPPLL_CLK_SRC = 1, the SN65DSIX6 will update the CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE with a value that represents the selected DSI clock frequency. Software can change this value.
(2) REFCLK pin must be tied or pull-down to GND when the DACP/N is used as the clock source for the DPPLL.
(3) If GPIO selection of REFCLK or DACP/N frequency is not used, then software must program the REFCLK_FREQ, CHA_DSI_CLK_RANGE and CHB_DSI_CLK_RANGE through the I2C interface prior to issuing any DSI commands or packets to the SN65DSIX6.

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### SUSPEND

The SUSPEND functionality is intended to be used with the Panel Self Refresh (PSR) feature of the eDP Sink. The PSR feature is intended for saving system power but this power saving must not produce any noticeable display artifacts to the end user. The de-assertion of EN will produce the greatest DSIX6 power savings but the reconfiguration of the DSIX6 may be too slow and therefore produce a bad end user experience. In this case, the SUSPEND feature is the next option for reducing DSIX6 power consumption while in an active PSR state. The SUSPEND features allows for quick exit from an active PSR state.

When the GPIO1 is configured for SUSPEND, if the SUSPEND (GPIO1) pin is asserted, then the DSIX6 will be placed in a low-power mode. The SUSPEND (GPIO1) pin will be sampled by the rising edge of REFCLK. If SUSPEND is sampled asserted, then all CSR registers will NOT get reset to their default values, and the DP PLL, DP interface, and DSI interfaces will be powered off. REFCLK can be turned off when DSIX6 is in the SUSPEND Mode.

The DSIX6 supports assertion of IRQ for HPD events. When an IRQ_HPD event is detected and both IRQ_EN and IRQ_HPD_EN bits are set, then the DSIX6 will assert the IRQ.

In order to take the DSIX6 out of the SUSPEND mode, the REFCLK must be running before and after the SUSPEND (GPIO1) pin is de-asserted. After the DP PLL is locked, the DSIX6 will transition the ML_TX_MODE from Main Link Off to either Normal or Semi-Auto Link depending on the state of PSR_TRAIN register. If the PSR_EXIT_VIDEO bit is set, then active video will begin transmitting over the DisplayPort interface after the first VSS (Vertical Sync Start) is detected on the DSI interface. If the PSR_EXIT_VIDEO bit is not set, software must enable the VSTREAM_ENABLE bit. Then active video will begin transmitting over the DisplayPort interface after the first VSS (Vertical Sync Start) is detected on the DSI interface.

**NOTE**

If the GPIO4_CTRL is configured for PWM, the PWM will be active during SUSPEND. If the system designer does not wish the PWM active during SUSPEND, then software can change the GPIO4_CTRL to Input before entering SUSPEND and then re-enable PWM after exiting SUSPEND by changing the GPIO4_CTRL to PWM.

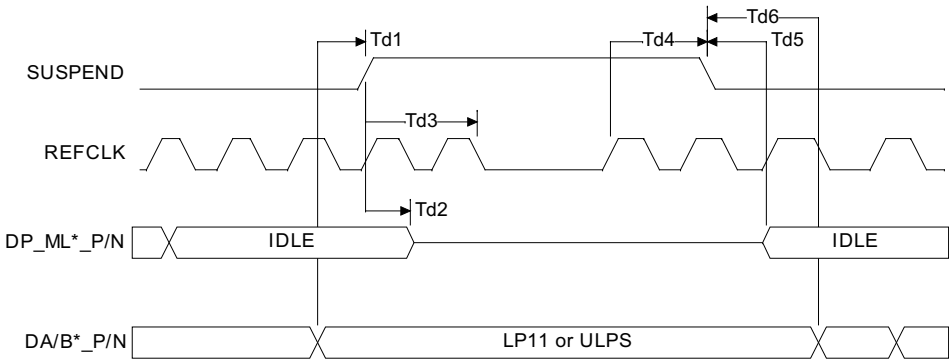


**Table 11. SUSPEND Timing Requirements**

| PARAMETER | DESCRIPTION | MIN | MAX |
|---|---|---|---|
| Td1 | LP11 or ULPS on DSI channel A and B before assertion of SUSPEND. | 200 ns | |
| Td2 | Delay from SUSPEND asserted to DisplayPort Main Link powered off. | 2 × $T_{REFCLK}$ | |
| Td3 | REFCLK active hold time after assertion of SUSPEND | 4 × $T_{REFCLK}$ | |
| Td4 | REFCLK active setup time before de-assertion of SUSPEND. | 100 ns | |
| Td5 | Delay from SUSPEND de-asserted to DisplayPort Main Link active and transmitting IDLE pattern. Semi-Auto Link Training is NOT used. | | 20µs + (1155 × $T_{REFCLK}$) |
| Td6 | LP11 state or ULPS on DSI channels A and B after SUSPEND de-assertion | 20µs + (1155 × $T_{REFCLK}$) | |

**NOTE**

For the case when DPPLL_CLK_SRC = 1, REFCLK mentioned in this section is replaced with a divided down version of the DSIA_CLK (DCAP/N). The means that DSIA_CLK must be active before the assertion of SUSPEND and before the de-assertion of SUSPEND as specified in Table 11. The DSIA_CLK can be stopped while in SUSPEND as long as above requirements are meet.

### Pulse Width Modulation (PWM)

The SN65DSIX6 supports controlling the brightness of eDP Display via pulse width modulation. The PWM signal is output over GPIO4 when GPIO4 control register is configured for PWM. For the SN65DSI86, the brightness is controlled by the BACKLIGHT register.

For the SN65DSI96, the brightness is controlled by either the BACKLIGHT register or the BACKLIGHT_OUT register. The OPTION_SELECT register determines which register is used. When OPTION_SELECT is set to zero, then BACKLIGHT_OUT is used to control the brightness. When OPTION_SELECT is not set to zero, then BACKLIGHT register is used to control brightness.

The granularity of brightness is controlled directly by the 16-bit BACKLIGHT_SCALE register. This register allows a granularity of up to 65535 increments. This register, in combination with either the BACKLIGHT or BACKLIGHT_OUT register, will determine the duty cycle of the PWM. For example, if the BACKLIGHT_SCALE register is programmed to 0xFF and the BACKLIGHT is programmed to 0x40, then the duty cycle will be 25% (25% of the PWM period will be high and 75% of the PWM period will be low). The duty cycle would be 100% (PWM always HIGH) if the BACKLIGHT register was programmed to 0xFF and would be 0% (PWM always low) if BACKLIGHT register was programmed to 0x00. The BACKLIGHT_SCALE should be set equal to the digital value corresponding to the maximum possible backlight brightness that the display can produce. For example, if the backlight level is 16-bit, then BACKLIGHT_SCALE should be 0xFFFF, if it is an 8-bit range, then BACKLIGHT_SCALE should be set to 0x00FF.

Duty Cycle (high pulse) = (BACKLIGHT or BACKLIGHT_OUT) / (BACKLIGHT_SCALE +1)

The frequency of the PWM is determined by the REFCLK_FREQ register and the value programmed into both the PWM_PRE_DIV and BACKLIGHT_SCALE registers. The equation below determines the PWM frequency:

PWM FREQ = REFCLK_FREQ / (PWM_PRE_DIV × BACKLIGHT_SCALE + 1)

Regardless of the state of the DPPLL_CLK_SRC register, the REFCLK_FREQ value in above equation will be based on the frequencies of DPPLL_CLK_SRC equal 0 (12MHz, 19.2MHz, 26MHz, 27MHz, 38.4MHz). The REFCLK_FREQ will not be the DSIA CLK frequency in the case where DPPLL_CLK_SRC equals one.

**NOTE**

REFCLK or DACP/N must be running if GPIO4 is configured for PWM.

**Table 12. PWM BACKLIGHT SELECTION OPTIONS**

| DSI86 | DSI96 | ADEN(1) | OPTION_SELECT(1) | PWM (GPIO4) |
|---|---|---|---|---|
| 1 | 0 | X | X | BACKLIGHT |
| 0 | 1 | 0 | X | BACKLIGHT |
| 0 | 1 | 1 | 0 | BACKLIGHT_OUT |
| 0 | 1 | 1 | Non-zero | BACKLIGHT |

(1) ADEN and OPTION_SELECT are only used for SN65DSI96.

## DISPLAYPORT

The SN65DSIX6 supports Single-Stream Transport (SST) mode over 1, 2, or 4 lanes at a datarate of 1.62Gbps, 2.16Gbps, 2.43Gbps, 2.7Gbps, 3.24Gbps, 4.32Gbps, or 5.4Gbps. The SN65DSIX6 does not support Multi-Stream Transport (MST) mode.

### HPD (Hot Plug/Unplug Detection)

The HPD signal is used by a DisplayPort source (DSIX6) for detecting when a downstream port (DisplayPort Panel) is attached or removed as well as for link status information. The [EDP] specification states that the HPD signal is required for an eDP Panel but is optional for a eDP source (DSIX6). The DSIX6 supports the HPD signal. It is up to the system implementer to determine if HPD signal is needed for the DSIX6. If not used, the system implementer should pull-up HPD to 3.3V or set the HPD_DISABLE bit. If HPD_DISABLE is set, then all HPD events (IRQ_HPD, HPD_REMOVAL, HPD_INSERTION, HPD_REPLUG) are disabled.

When IRQ_EN and IRQ_HPD_EN is enabled, the DSIX6 will assert the IRQ whenever the eDP generates a IRQ_HPD event. An IRQ_HPD event is defined as a change from INSERTION state to the IRQ_HPD state.

The DSIX6 will also interpret a DisplayPort device removal or insertion as an HPD_REMOVAL or HPD_INSERTION event. A HPD_REMOVAL event is defined as a change that causes the HPD state to transition from INSERTION state to the REMOVAL state. A HPD_INSERT event is defined as a change that causes the HPD state to transition from the REMOVAL state to the INSERTION state. The REPLUG event is caused by the sink de-asserting HPD for more than 2ms but less than 100ms. If software needs to determine the state of the HPD pin, it should read the HPD Input register. The HPD state machine operates off an internal ring oscillator. The ring oscillator frequency will vary based on PVT (process voltage temperature). The min/max range in the HPD State Diagram refers to the possible times based off variation in the ring oscillator frequency.

**NOTE**

HPD has a minimum of 60 kΩ ± 15% internal pull-down resistor.

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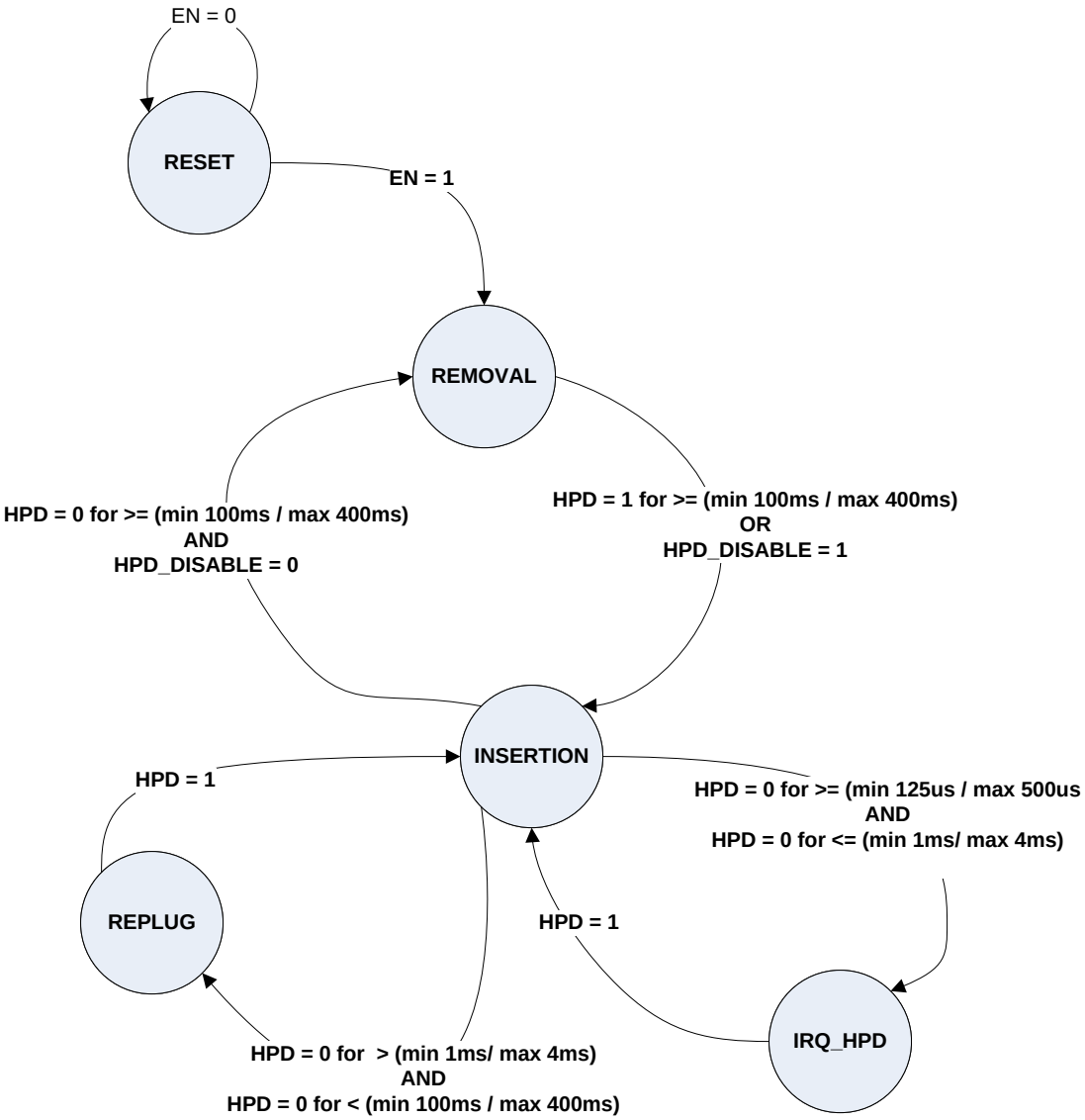


**Figure 15. HPD State Diagram**

### AUX_CH

The AUX_CH supported by the DSIX6 is a half-duplex, bidirectional, ac-coupled, doubly-terminated differential pair. Manchester-II coding is used as the channel coding for the AUX_CH and supports a datarate of 1Mbps. Fast AUX (aka FAUX) is not supported by the DSIX6. Over the AUX_CH, the DSIX6 will always transmit the most significant bit (msb) first and the least significant bit (lsb) last. Bit 7 is the msb and Bit 0 is the lsb.

The purpose of the AUX_CH is to provide a side-band channel between the DSIX6 and the downstream eDP device. Through the AUX_CH, the following is some of the information which can be obtained from or provided to the downstream eDP device

1. eDP Downstream DPCD capabilities (# of lanes, datarate, display authenticate method, etc…)
2. EDID information of display like native resolution (obtained by I2C over AUX transactions)
3. Link training and status
4. MCCS control

### *Native Aux Transactions*

Native Aux transaction is broken into two pieces: Request and Reply. The DSIX6 will always be the originator of the Request (sometimes under GPU control and other times under DSIX6 HW control) and the recipient of the Reply from the downstream device.

Request Syntax: <4-bit AUX_CMD> <20-bit AUX_ADDR> <7-bit AUX_LENGTH> <DATA0 … DATA15>

Reply Syntax: <4-bit AUX_CMD> <4'b0000> <DATA0 … DATA15>

**Table 13. Definition of the AUX_CMD Field for Request Transactions**

| AUX_CMD[3:0] | DESCRIPTION |
|---|---|
| 0x0 | I2C-Over-Aux Write MOT = 0. |
| 0x1 | I2C-Over-Aux Read MOT = 0 |
| 0x2 | I2C-Over-Aux Write Status Update MOT = 0. |
| 0x3 | Reserved. DSIX6 will ignore. |
| 0x4 | I2C-Over-Aux Write MOT = 1 |
| 0x5 | I2C-Over-Aux Read MOT = 1 |
| 0x6 | I2C-Over-Aux Write Status Update MOT=1. |
| 0x7 | Reserved. DSIX6 will ignore. |
| 0x8 | Native Aux Write |
| 0x9 | Native Aux Read |
| 0xA – 0xF | Reserved. DSIX6 will ignore. |

For Native Aux Reply transactions, the DSIX6 will update the status field in the CFR with command provided by the eDP device. For example, if the eDP receiver replies with a AUX_DEFER, the DSIX6 will attempt the request seven times (100µs between each attempt) before updating the AUX_DEFR status field with 1'b1. If the eDP receiver does NOT reply before the 400-us reply timer times-out, then the DSIX6 will wait 100µs before trying the request again. The DSIX6 will retry the request seven times before giving up and then update the AUX_RPLY_TOUT field with 1'b1.

Example: Native Aux read of the eDP receiver capability field at DCPD address 0x00000h thru 0x00008

1. Software program the AUX_CMD field with 0x9.
2. Software program the AUX_ADDR[19:16] field with 0x0.
3. Software program the AUX_ADDR[15:8] field with 0x0.
4. Software program the AUX_ADDR[7:0] field with 0x0.
5. Software program the AUX_LENGTH field with 0x8.
6. Software set the SEND bit.
7. DSIX6 will transmit the following packet: <SYNC> <0x90> <0x00> <0x00> <0x07> <STOP>
8. Within 300µs, the eDP receiver will reply with the following: <SYNC> <0x00> <DATA0> <DATA1> <DATA2> <DATA3> <DATA4> <DATA5> <DATA6> <DATA7> <STOP>
9. DSIX6 will update AUX_RDATA0 thru AUX_RDATA7 with the data received from the eDP receiver.
10. DSIX6 will update the AUX_LENGTH field with 0x8 indicating eight bytes we received.
11. DSIX6 will then clear the SEND bit.
12. If enabled, the IRQ will get asserted to indicate to GPU that the Native Aux Read completed.
13. GPU should read from the Interrupt Status register to see if the Native Aux Read completed successfully.

### I2C-Over-AUX

There are two methods available for I2C-Over-Aux: Direct Method (aka Clock stretching) and Indirect Method (CFR Read/Write).

### *Direct Method (Clock Stretching)*

The Direct Method (Clock Stretching) involves delaying the acknowledge or data to the $I^2C$ Master by the DSIX6 driving the SCL pin low. Once the DSIX6 is ready to acknowledge an $I^2C$ write transaction or return read data for a I2C read transaction, the DSIX6 will tri-state the SCL pin therefore allowing the acknowledge cycle to complete.

In order to enable the Direct Method (Clock Stretching) software must do the following:

1. Program the 7-bit $I^2C$ slave address(s) into the I2C_ADDR_CLAIMx register(s).
2. Enable Direct Method by setting the I2C_CLAIMx_EN bit(s).

### *Indirect Method (CFR Read/Write)*

The Indirect Method is intended to be used by a GPU which does NOT support the Direct Method (Clock Stretching). The Indirect Method involves programming the appropriate CFR registers. The Indirect Method is very similar to the Native Aux method described above.

Example of Indirect $I^2C$ Read of the EDID.

1. Program the AUX_CMD = 0x4, AUX_ADDR[7:0] = 0x50, and AUX_LENGTH = 0x00.
2. Set the SEND bit.
3. The DSIX6 will clear the SEND bit once the Request has been ACKed.
4. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 5.
5. Program the AUX_CMD = 0x4, AUX_ADD[7:0] = 0x50, AUX_LENGTH = 0x01, and AUX_WDATA0 = 0x00.
6. Set the SEND bit.
7. The DSIX6 will clear the SEND bit once the Request has been ACKed.
8. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 9.
9. Program the AUX_CMD = 0x5, AUX_ADDR[7:0] = 0x50, and AUX_LENGTH = 0x00.
10. Set the SEND bit.
11. The DSIX6 will clear the SEND bit once the Request has been ACKed.
12. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 13.
13. Program the AUX_CMD = 0x5, AUX_ADDR[7:0] = 0x50, and AUX_LENGTH = 0x10.
14. Set the SEND bit.
15. The DSIX6 will clear the SEND bit once the Request has been ACKed.
16. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag, read data from AUX_RDATA0 thru AUX_DATA15, and go to step 13.
17. If read of EDID is complete, the go to step 18. If read of EDID is not complete, then go to Step 13.
18. Program the AUX_CMD = 0x1, AUX_ADDR[7:0] = 0x50, and AUX_LENGTH = 0x00.
19. Set the SEND bit.
20. The DSIX6 will clear the SEND bit once the Request has been ACKed.
21. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 22.
22. Read of EDID finished.

Example of an indirect I2C Write (Changing EDID Segment Pointer):

1. Program the AUX_CMD=0x4, AUX_ADDR[7:0]=0x30, and AUX_LENGTH=0x00.
2. Set the SEND bit.
3. The DSIX6 will clear the SEND bit once the Request has been ACKed.
4. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 5.
5. Program the AUX_CMD=0x4, AUX_ADDR[7:0]=0x30, AUX_LENGTH=0x01, and AUX_WDATA0 = 0x01.
6. Set the SEND bit.

7. The DSIX6 will clear the SEND bit once the Request has been ACKed.
8. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 9.
9. Program the AUX_CMD=0x0, AUX_ADDR[7:0]=0x30, and AUX_LENGTH=0x00.
10. Set the SEND bit.
11. The DSIX6 will clear the SEND bit once the Request has been ACKed.
12. If SEND_INT_EN is enabled and IRQ_EN is enabled, an IRQ will be asserted. GPU should make sure no error flags are set. If no error flags are set, GPU should clear the SEND_INT flag and go to step 13.
13. Finished.

The DSIX6 will handle all aspects of completing a request I2C-Over-Aux Read or Write. Once the requested Read or Write completes, the DSIX6 will clear the SEND bit and if an error occurred, the DSIX6 will set the NAT_I2C_FAILED flag. The NAT_I2C_FAILED flag will get set if for some reason the slave NACK the I2C Address. If the Slave NACK without completing the entire request AUX_LENGTH, the DSIX6 will set the AUX_SHORT flag and update the AUX_LENGTH register with the amount of data completed and then clear the SEND bit. Upon clearing the SEND bit and if IRQ assertion is enabled, the DSIX6 will assert IRQ.

### DisplayPort PLL

By default, the DisplayPort PLL is disabled (DP_PLL_EN = 0). In order to perform any operations over the DisplayPort Main link interface, the DP_PLL_EN must be enabled. Before enabling the DisplayPort PLL, software must program the DP_DATARATE register with the desired datarate. Also if SSC is going to be used, the SSC_ENABLE and SSC_SPREAD should also be programmed. Once the DP_PLL_EN is programmed to 1, software should wait until the DP_PLL_LOCK bit is set before performing any DisplayPort Main Link operations.

Depending on DSIX6 configuration, the amount of time for the DP PLL to lock will vary. Table 14 describes the lock times for various configurations.

**Table 14. DP_PLL Lock Times**

| REFCLK_FREQ | SSC_ENABLE | Maximum Lock Time |
|---|---|---|
| 0 | X | 20 µs + (1152 × $T_{REFCLK}$) |
| 1 | X | |
| 2 | X | |
| 4 | X | |
| 3 | 1 | |
| 3 | 0 | 20 µs + (128 × $T_{REFCLK}$) |

## 7.4 DP Output VOD and Pre-emphasis Settings

The DSIX6 has user configurable VOD, pre-emphasis, and post-cursor2 levels. The post cursor 2 level is defined by the DP_POST_CURSOR2 level. The VOD and pre-emphasis levels are defined by the *DP Link Training Lookup Table*. The defaults settings from this lookup table are described in Table 15.

**Table 15. Pre-Emphasis Default Settings**

| | PRE-EMPHASIS | | | |
|---|---|---|---|---|
| **VOD LEVEL** | **LEVEL 0** | **LEVEL 1** | **LEVEl 2** | **LEVEL 3** |
| Level 0 (400 mV) | Enabled (0 dB) | Enabled (3.74 dB) | Enabled (6.02 dB) | Disabled |
| Level 1 (600 mV) | Enabled (0 dB) | Enabled (3.10 dB) | Enabled (5.19 dB) | Disabled |
| Level 2 (800 mV) | Enabled (0 dB) | Enabled (2.50 dB) | Disabled | Disabled |
| Level 3 | Disabled | Disabled | Disabled | Disabled |

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All of these default values can be changed by modifying the values in the DP Link Training Lookup Table

## DP Main Link Configurability

The SN65DSIX6 has four physical DisplayPort lanes and each physical lane can be assigned to one specific logical lane. By default, physical lanes 0 thru 3 are mapped to logical lanes 0 thru 3. When routing between the SN65DSIX6 and a non-standard eDP receptacle, the physical to logical lane mapping can be changed so that PCB routing complexity is minimized. Table 16 depicts the supported logical to physical combinations based on the number of lanes programmed into the DP_NUM_LANES registers.

**Table 16. Logical to Physical Supported Combinations**

| DP_NUM_LANES | LN0_ASSIGN | LN1_ASSIGN | LN2_ASSIGN | LN3_ASSIGN |
|---|---|---|---|---|
| 1 | 0 or 1. 0 is recommended. | | | |
| 2 | 0 or 1 | 0 or 1 | | |
| 4 | 0, 1, 2, or 3 | 0, 1, 2, or 3 | 0, 1, 2, or 3 | 0, 1, 2, or 3 |

Note the DSIX6's DisplayPort logic uses clocks from physical lane 0, and therefore these clocks from physical lane 0 will be active whenever the DP PLL is enabled. When using less than four DP lanes, the optimal power consumption is achieved by always using physical lane 0.

## DP Main Link Training

The DSIX6 supports four methods to train the DisplayPort link:

1. Manual Training
2. Fast Training
3. Semi Auto Training
4. Redriver Semi Auto Training

Note it is software responsibility to enable the Display Authentication Method in the eDP Display before any link training can be performed. The DSIX6 is enabled for ASSR authentication method by default. The DSIX6 supports Enhanced Framing. If the eDP panel supports DPCD Revision 1.2 or higher, software must enable the Enhanced Framing Mode.

### Manual Link Training

This method is completely under software control. Software is required to handle the entire link training process.

### Fast Link Training

In order the use the Fast Training method, there must be prior knowledge of the eDP receiver capabilities. Software must program both the DSIX6 and the eDP receiver with pre-calibrated parameters (DP_TX_SWING, DP_PRE_EMPHASIS, DP_NUM_LANES, and DP_DATARATE). Upon completing the programming of the pre-calibrated settings, software must transition the ML_TX_MODE to Fast Link Training. If TPS1 during Fast Link Training is enabled, DSIX6 will then transmit the clock recovery pattern (TPS1) for at least 500us and then transition ML_TX_MODE to normal. If TPS2 during Fast Link training is enabled, then after the TPS1, the DSIX6 will transmit TPS2 for 500us before transitioning ML_TX_MODE to normal. If neither TPS1 nor TPS2 during Fast Link Training is enabled, then the DSIX6 will transition straight to normal mode.

**NOTE**

GPU should determine if the eDP Display supports Fast Link training by reading the NO_AUX_HANDSHAKE_LINK_TRAINING bit at DCPD address 0x00003 bit 6. If this bit is set, then the eDP Display supports Fast Link Training.

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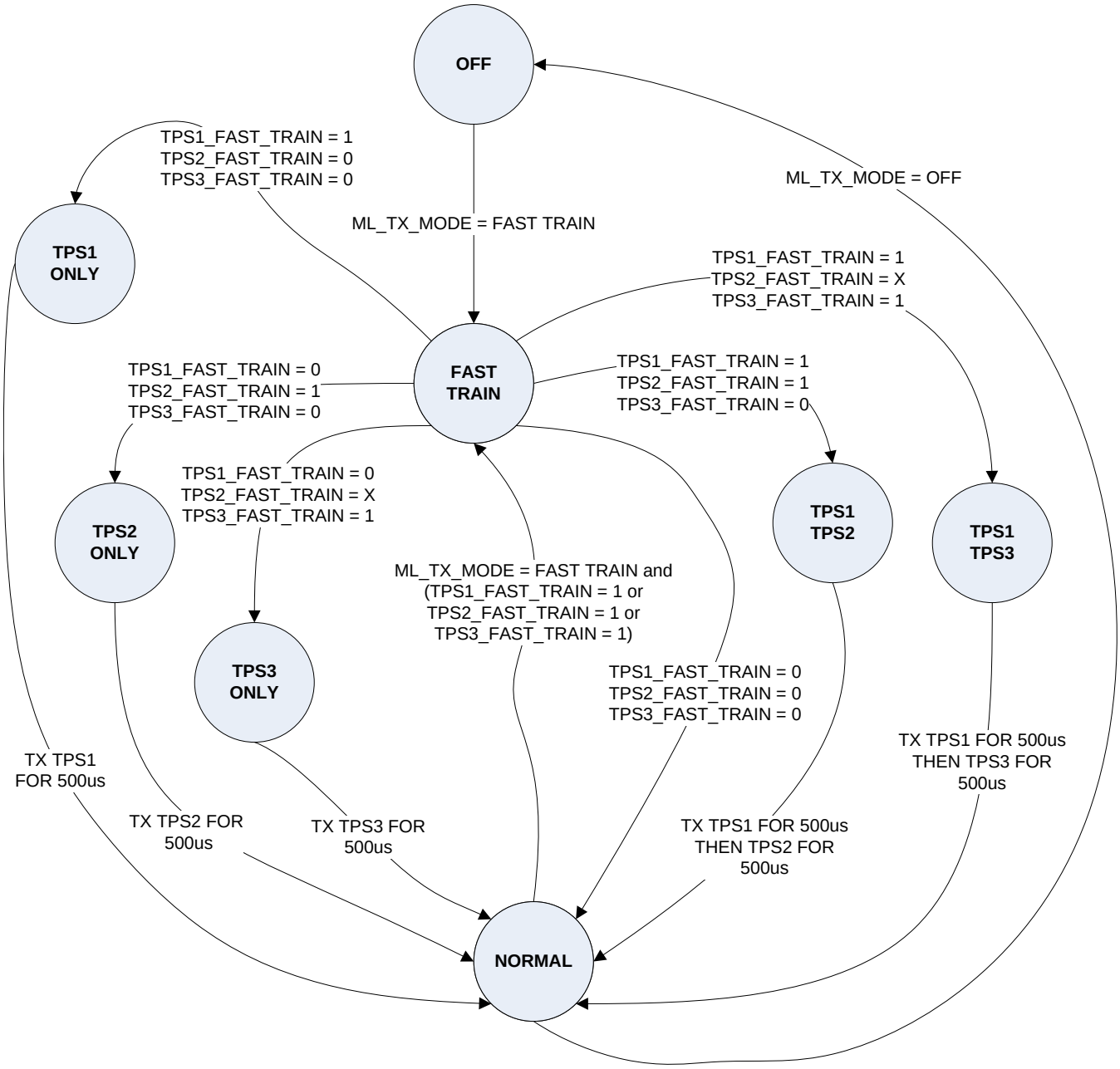


**Figure 16. Fast-Link Training State Diagram**

### Semi Auto Link Training

In order to use the semi auto link training mode, software must first program the target DP_NUM_LANES and DP_DATARATE. Once these fields have been programmed, software can then transition the ML_TX_MODE to Semi Auto Link Training. The DSIX6 will then attempt to train the DisplayPort link at the specified datarate and number of lanes. The DSIX6 will try all possible combinations of DP_PRE_EMPHASIS and DP_TX_SWING. Training will end as soon as a passing combination is found or all combinations have been tried and failed. The possible combinations are determined by the setting in the *DP Link Training LUT registers*. If training is successful, the DSIX6 will update the DP_POST_CURSOR2, DP_PRE_EMPHASIS, and DP_TX_SWING with

the passing combination and then transition the ML_TX_MODE to normal. If training is unsuccessful, the DSIX6 will transition the ML_TX_MODE to Main Link Off. If enabled, the DSI will assert the IRQ pin whether or not training was successful. Software will then need to specify a different target DP_NUM_LANES and DP_DATARATE and then transition the ML_TX_MODE to Semi Auto Link Training. This process is repeated until successful link training occurs.

**NOTE**

Once software has enabled Semi-Auto Linking training, software must wait for the training to complete before performing any AUX transactions (Native Aux or I2C-Over-Aux).

### Redriver Semi Auto Link Training

In some systems a DisplayPort redriver (like the DP130) would sit between the SN65DSIX6 and the eDP panel. In these applications, it is important to train the DisplayPort link between the DSIX6 and the redriver to one setting and training the link between the redriver and the eDP panel to a different setting. For this application, Redriver Semi Auto Link training can be used.

Redriver Semi Auto Link training is essentially the same as Semi Auto Link training with one major difference. That difference is Redriver Semi Auto Link Training will never change the DP_TX_SWING, DP_PRE_EMPHASIS, and DP_POST_CURSOR2 levels being driven by the SN65DSIX6. These settings will always stay fixed to their programmed values. The SN65DSIX6 will still send all aux requests to the eDP panel's DPCD registers. The redriver will snoop these aux transactions and train the link between it and the eDP panel.

## Panel Size vs DP Configuration

Table 17 is provided as a guideline of the best DP configuration (datarate and number of lanes) for a specific video resolution and color depth. The preferred (P) setting assumes the eDP panel supports the 5.4Gbps datarate.

**Table 17. Recommended DP Configuration**

| Common Video Mode Name | VESA Timing Name (Horizontal x Vertical at Frame Rate) | Pixel Clock Rate (MHz) | RGB666 | | | | RGB888 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Stream Bit Rate (Gbps) | Required Number of DP Lanes at | | | Stream Bit Rate (Gbps) | Required Number of DP Lanes at | | |
| | | | | 1.62Gbps | 2.7Gbps | 5.4Gbps | | 1.62Gbps | 2.7Gbps | 5.4Gbps |
| XGA | 1024x768 @ 60Hz CVT (Reduced Blanking) | 56 | 1.01 | 1 (P) | 1 | 1 | 1.34 | 2 | 1 (P) | 1 |
| WXGA | 1280x768 @ 60Hz CVT (Reduced Blanking) | 68 | 1.23 | 1 (P) | 1 | 1 | 1.64 | 2 | 1 (P) | 1 |
| WXGA | 1280x800 @ 60Hz CVT (Reduced Blanking) | 71 | 1.28 | 1 (P) | 1 | 1 | 1.7 | 2 | 1 (P) | 1 |
| HD | 1366x768 @ 60Hz | 86 | 1.54 | 2 | 1 (P) | 1 | 2.05 | 2 | 1 (P) | 1 |
| WXGA+ | 1440x900 @ 60Hz CVT (Reduced Blanking) | 89 | 1.6 | 2 | 1 (P) | 1 | 2.13 | 2 | 1 (P) | 1 |
| SXGA+ | 1400x1050 @ 60Hz CVT (Reduced Blanking) | 101 | 1.82 | 2 | 1 (P) | 1 | 2.42 | 2 | 2 | 1 (P) |
| HD+ | 1600x900 @ 60Hz (Reduced Blanking) | 108 | 1.94 | 2 | 1 (P) | 1 | 2.59 | 4 | 2 | 1 (P) |
| WSXGA+ | 1680x1050 @ 60Hz CVT (Reduced Blanking) | 119 | 2.12 | 2 | 1 (P) | 1 | 2.86 | 4 | 2 | 1 (P) |
| UXGA | 1600x1200 @ 60Hz CVT (Reduced Blanking) | 130 | 2.34 | 2 | 2 | 1 (P) | 3.13 | 4 | 2 | 1 (P) |
| FHD | 1920x1080 @ 60Hz | 149 | 2.67 | 4 | 2 | 1 (P) | 3.56 | 4 | 2 | 1 (P) |
| WUXGA | 1920x1200 @ 60Hz CVT (Reduced Blanking) | 154 | 2.77 | 4 | 2 | 1 (P) | 3.7 | 4 | 2 | 1 (P) |
| WQXGA | 2560x1600 @60Hz CVT (Reduced Blanking) | 269 | 4.83 | 4 | 4 | 2 (P) | 6.44 | NA | 4 | 2 (P) |

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## Panel Self Refresh (PSR)

The Panel Self Refresh feature enables system-level power savings when the displayed image remains static for multiple display frames. The eDP display (Sink) stores a static image locally in a remote frame buffer (RFB) within the sink and displays this image from the RFB while the eDP Main link may be turned off (SUSPEND asserted). The DSIX6 may turn off other features in addition to the main link for further power savings. The system software makes the determination on what power savings shall be implemented (like shutdown of DP link (SUSPEND asserted), shutdown of entire DSIX6 (EN de-asserted), etc.). When implementing PSR, any power savings must not impact system responsiveness to user input that affects the display, such as cursor movement.

The list below are the requirements the GPU and system designer must meet when implementing PSR:

1. Updates to the remote frame buffer located in sink must include two of the same static frame. The reason for this requirement is the DSIX6 will never pass the first frame received on the DSI interface to the DisplayPort interface. All subsequent frames will be passed to the DisplayPort interface.
2. If PWM signal is controlled directly by the DSIX6 and SUSPEND asserted, the REFCLK must remain active.
3. Changes in ambient light level must be relayed to the DSI96 along with updates to the remote frame buffer in the sink.
4. Sink CRC verification must be disabled when the Assertive Display core is enabled. (applies only to the SN65DSI96)

## Secondary Data Packet (SDP)

All secondary data packets (SDP) are provided to the DSIX6 through the DSI interface during vertical blanking periods. (SDP are not supported using the I2C interface). The DSIX6 will wrap the SDP provided to the DSI interface with the SS and SE control symbols and then transmit over the DP interface during the vertical blanking period. Secondary data packets are used to pass non-active video data to the eDP sink. Information like stereo video attributes and/or PSR-state data is sent using SDP. When SDP is used for stereo video attributes, software must program the MSA_MISC1_2_1 register with a zero.

The DSIX6 requires that the SDP be provided to the DSI interface in the following order:

1. 4 Bytes of Header (HB0 thru HB3)
2. 4 Bytes of Header parity (PB0 thru PB3)
3. 8 Bytes of Data (DB0 thru DB7)
4. 2 Bytes of Data parity (PB4 and PB5)
5. 8 Bytes of Data {DB8 thru DB15)
6. 2 Bytes of Data parity (PB6 and PB7)

For data payloads greater than 16 bytes, data must be provided in multiples of 8 bytes with of 2 bytes of parity. If the final multiple is less than 8, zero padding must be used to fill the remaining data positions.

## Color Bar Generator

The DSIX6 implements a SMPTE color bar. The color bar generator does not require the DSI interface. All color bars will be transmitted at a 60Hz frame rate. The active video size of the Color bar is determined by the values programmed into the Video Registers.

The color bar generator supports the following color bars for both horizontal and vertical direction:

1. 8 color {White, Yellow, Cyan, Green, Magenta, Red, Blue, Black}
2. 8 gray scale {White, Light Gray, Gray, Light Slate Gray, Slate Gray, Dim Gray, Dark Slate Gray, Black}
3. 3 color {Red, Green, Blue}
4. Stripes {White, Black}. Every other pixel (pixel1 = white, pixel2 = black, pixel3 = white, etc...).

**Table 18. 24-bit RGB Color Codes**

| Color | Red | Green | Blue |
|---|---|---|---|
| Black | 0x00 | 0x00 | 0x00 |
| Red | 0xFF | 0x00 | 0x00 |
| Green | 0x00 | 0xFF | 0x00 |
| Blue | 0x00 | 0x00 | 0xFF |
| Yellow | 0xFF | 0xFF | 0x00 |
| White | 0xFF | 0xFF | 0xFF |
| Magenta | 0xFF | 0x00 | 0xFF |
| Cyan | 0x00 | 0xFF | 0xFF |
| Gray | 0xBE | 0xBE | 0xBE |
| Light Gray | 0xD3 | 0xD3 | 0xD3 |
| Light Slate Gray | 0x77 | 0x88 | 0x99 |
| Slate Gray | 0x70 | 0x80 | 0x90 |
| Dim Gray | 0x69 | 0x69 | 0x69 |
| Dark Slate Gray | 0x2F | 0x4F | 0x4F |

**NOTE**

Both VSTREAM_ENABLE and Color_Bar_En must be set in order to transmit Color Bar over DisplayPort interface. Also, ML_TX_MODE must be programmed to Normal Mode.



## DP Pattern

DSIX6 supports the training and compliance patterns mentioned in Table 19. The value of ML_TX_MODE register controls what pattern will be transmitted.

**Table 19. DP Training and Compliance Patterns**

| PATTERN | [DP] SECTION |
|---|---|
| IDLE | 5.1.3.1 |
| TPS1 | Table 3-16 and 2.9.3.6.1 |
| TPS2 | Table 3-16 |
| TPS3 | Table 3-16 |
| PRBS7 | Table 2-75 address 0x00102. |
| HBR2 Compliance Eye(1) | 2.9.3.6.5 |
| Symbol Error Rate Measurement(1) | 2.9.3.6.2 and 2.10.4 |
| 80 bit Customer Pattern | 2.9.3.6.4 |

(1) HBR2 Compliance Eye and Symbol Error Rate Measurement require TEST2 pin to be pulled up before the assertion of EN and software program a '1' to bit 0 of offset 0x16 at Page 7 followed by a write of '0' to bit 0 of offset 0x5A at Page 0 before writing either a 0x6 or 0x7 to ML_TX_MODE register.

### HBR2 Compliance Eye

When the ML_TX_MODE is set to HBR2 Compliance Eye, the SN65DSIX6 will use the value programmed into the HBR2_COMPEYEPAT_LENGTH register to determine the number of scrambled 0 before transmitting an Enhanced Frame Scrambler Reset sequence. The Enhanced Framing Scrambler Reset sequence used is determined by ENCH_FRAME_PATT register.

**Table 20. Common 80-bit Custom Patterns**

| Byte# | PLTPAT | PCTPAT |
|---|---|---|
| 0 | 0x1F | 0x1F |
| 1 | 0x7C | 0x7C |
| 2 | 0xF0 | 0xF0 |
| 3 | 0xC1 | 0xC1 |
| 4 | 0x07 | 0xCC |
| 5 | 0x1F | 0xCC |
| 6 | 0x7C | 0xCC |
| 7 | 0xF0 | 0x4C |
| 8 | 0xC1 | 0x55 |
| 9 | 0x07 | 0x55 |

### 80-Bit Custom Pattern

The 80-bit Custom pattern is used for generating the Post Cursor2 Test Pattern (PCTPAT) and the Pre-Emphasis Level Test Pattern (PLTPAT). The SN65DSIX6 will continuously transmit the value programmed into the *80BIT_CUSTOM_PATTERN* registers when the ML_TX_MODE is programmed to 80-bit Custom Pattern. The SN65DSIX6 will always transmit over the enabled DisplayPort Lanes the lsb of the byte first and the msb of the byte last. The byte at the lowest address is transmitted first.

## BPP Conversion

The SN65DSIX6 transmits either 18bpp or 24bpp over the DisplayPort interface based on the DP_18BPP_EN bit. When this bit is cleared and 18bpp is being received on DSI interface, the SN65DSIX6 performs the following translation of the 18bpp into 24bpp: new[7:0] = {original[5:0], original[5:4]}. When the DP_18BPP_EN bit is set and 24bpp is being received on DSI interface, the SN65DSIX6 performs the following translation of 24bpp to 18bpp: new[5:0] = original[7:2].

## ASSERTIVE DISPLAY (SN65DSI96 ONLY)

Integrated into the SN65DSI96 is an adaptive content management and backlight control core called *Assertive Display*. The *Assertive Display* core's purpose is to optimize the viewing experience on a multimedia display as a function of viewing environment. It provides coherent management of the multimedia viewing experience from total darkness to bright ambient light conditions enabling the display to operate at reduced power and in bright sunshine.

The *Assertive Display* core achieves this via a combination of advanced pixel mapping and adaptive backlight control techniques. These techniques are based upon control algorithms that model the way the human eye adapts to changes both to the content displayed on the device and changes in the viewing environment, including the periphery of the visual field. The objective is to minimize the effect of these changes on the viewing experience perceived by the user.

The primary functions of the *Assertive Display* core are summarized in the table below:

| FUNCTION | DESCRIPTION |
|---|---|
| Backlight adaptation to ambient light | Calculates the optimal backlight value at a given ambient light level, based on a calibrated model of human eye adaptation to the ambient light environment. This ensures maximum viewing comfort and maximum display power consumption. |
| Content adaptation to ambient light | Adjusts the values of individual pixels in the video stream to match content dynamic range with screen contrast ratio under all viewing conditions. This ensures that content appearance is as close as possible to original content creator's intention. Furthermore, this enables multimedia viewing on standard emissive displays in bright sunshine. |
| Display power reduction | Enables adjustment of the display brightness profile to achieve large power savings while preserving a high-quality viewing experience. |
| Content adaptation to display contrast | In low-light viewing conditions, adapts multimedia content intended for use on displays with contrast ratio in excess of 5000:1 to the lower contrast ratio of a portable display. |

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| FUNCTION | DESCRIPTION |
|---|---|
| Content adaptation to field of view | Compensates for the limitation in human vision, specifically that contrast ratios in express of 100:1 cannot be resolved on small displays. |

Refer to the SN65DSI96 TRM for more details (operation, register set, etc…) on the Assertive Display core.

## LOCAL I²C INTERFACE OVERVIEW

The SN65DSIX6 local I²C interface is enabled when EN is input high, access to the CSR registers is supported during ultra-low power state (ULPS). The SCL and SDA terminals are used for I²C clock and I²C data respectively. The SN65DSIX6 I²C interface conforms to the two-wire serial interface defined by the I²C Bus Specification, Version 2.1 (January 2000), and supports fast mode transfers up to 400 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for SN65DSIX6 is factory preset to 010110X with the least significant bit being determined by the ADDR control input. Table 21 clarifies the SN65DSIX6 target address.

**Table 21. SN65DSIX6 I²C Target Address Description**

| SN65DSIX6 I²C TARGET Address | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (W/R) |
| 0 | 1 | 0 | 1 | 1 | 0 | ADDR | 0/1 |

When ADDR=1, Address Cycle is 0x5A (Write) and 0x5B (Read)

When ADDR=0, Address Cycle is 0x58 (Write) and 0x59 (Read)

The following procedure is followed to write to the SN65DSIX6 I2C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSIX6 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The master presents the sub-address (I²C register within SN65DSIX6) to be written, consisting of one byte of data, MSB-first
3. The master presents the sub-address ((I²C register within SN65DSIX6) to be written, consisting of one byte of data, MSB-first
4. The SN65DSIX6 acknowledges the sub-address cycle
5. The master presents the first byte of data to be written to the (I²C register
6. The SN65DSIX6 acknowledges the byte transfer
7. The master terminates the write operation by generating a stop condition (P)
8. The master terminates the write operation by generating a stop condition (P)

The following procedure is followed to read the SN65DSIX6 I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN65DSIX6 7-bit address and a one-value “W/R” bit to indicate a read cycle
2. The SN65DSIX6 acknowledges the address cycle
3. The SN65DSIX6 transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the SN65DSIX6 I2C register occurred prior to the read, then the SN65DSIX6 will start at the sub-address specified in the write.
4. The SN65DSIX6 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I2C master acknowledges reception of each data byte transfer
5. If an ACK is received, the SN65DSIX6 transmits the next byte of data
6. The master terminates the read operation by generating a stop condition (P)

The following procedure is followed for setting a starting sub-address for I2C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSIX6 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The SN65DSIX6 acknowledges the address cycle
3. The master presents the sub-address (I²C register within SN65DSIX6) to be written, consisting of one byte of data, MSB-first

4. The SN65DSIX6 acknowledges the sub-address cycle
5. The master terminates the write operation by generating a stop condition (P)

Note if no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the ($I^2C$ master terminates the read operation. If a I2C write occurred prior to the read, then the reads start at the sub-address specified by the write.

## CONTROL AND STATUS REGISTERS OVERVIEW

Many of the SN65DSIX6 functions are controlled by the Control and Status Registers (CSR). All CSR registers are accessible through the local $I^2C$ interface or through DSI interface.

Reads from reserved fields not described return zeros, and writes to read-only reserved registers are ignored. Writes to reserved register which are marked with 'W' will produce unexpected behavior.

**Table 22. Bit Field Access Tag Descriptions**

| ACCESS TAG | NAME | MEANING |
|---|---|---|
| R | Read | The field may be read by software |
| W | Write | The field may be written by software |
| S | Set | The field may be set by a write of one. Writes of zeros to the field have no effect. |
| C | Clear | The field may be cleared by a write of one. Write of zero to the field have no effect. |
| U | Update | Hardware may autonomously update this field. |
| NA | No Access | Not accessible or not applicable |

### Register Map

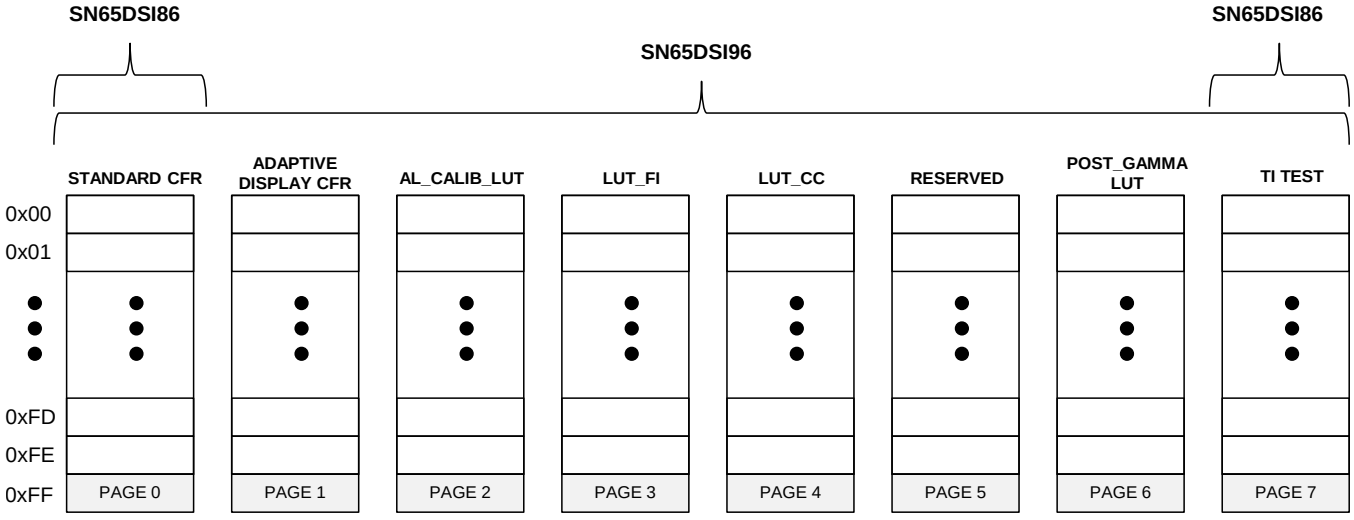


**Figure 17. Register Map**

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## Standard CFR Registers (PAGE 0)

### Table 23. CSR Bit Field Definitions – ID Registers

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x00 – 0x07 | 7:0 | DEVICE_ID<br>For the SN65DSI86 these fields return a string of ASCII characters returning “DSI86” preceded by three space characters.<br>Addresses 0x07 - 0x00 = {0x20, 0x20, 0x20, 0x44, 0x53, 0x49, 0x38, 0x36}<br>For the SN65DSI96 these fields return a string of ASCII characters returning “DSI96” preceded by three space characters.<br>Addresses 0x07 - 0x00 = {0x20, 0x20, 0x20, 0x44, 0x53, 0x49, 0x39, 0x36} | R |
| 0x08 | 7:0 | DEVICE_REV<br>Device revision; returns 0x02. | |

### Table 24. CSR Bit Field Definitions – Reset and Clock Registers

| ADDRESS | BIT(S) | DESCRIPTION | | ACCESS |
|---|---|---|---|---|
| 0x09 | 0 | SOFT_RESET<br>This bit automatically clears when set to ‘1’ and returns zeros when read. This bit must be set after the CSR’s are updated. This bit must also be set after making any changes to the DIS clock rate or after changing between DSI burst and non-burst modes.<br>0 – No action (default)<br>1 – Reset device to default condition excluding the CSR bits. | | W |
| 0x0A | 7 | DP_PLL_LOCK<br>0 – DP_PLL not locked (default)<br>1 – DP_PLL locked | | R |
| | 6:4 | Reserved | | R |
| | 3:1 | REFCLK_FREQ. This field is used to control the clock source and frequency select inputs to the DP PLL. Any change in this field will cause the DP PLL to reacquire lock. On the rising edge of EN the DSIX6 will sample the state of GPIO[3:1] as well as detect the presence or absence of a clock on REFCLK pin. The outcome will determine whether the clock source for the DP PLL is from the REFCLK pin or the DSIA CLK. The outcome will also determine the frequency of the clock source. | | RWU |
| | | DPPLL_CLK_SRC = 0 | DPPLL_CLK_SRC = 1 | |
| | | 000 – 12 MHz<br>001 – 19.2 MHz (Default)<br>010 – 26 MHz<br>011 – 27 MHz<br>100 – 38.4 MHz<br>All other combinations are 19.2 MHz | 000 – Continuous DSIA CLK at 468 MHz<br>001 – Continuous DSIA CLK at 384 MHz<br>010 – Continuous DSIA CLK at 416 MHz<br>011 – Continuous DSIA CLK at 486 MHz<br>100 – Continuous DSIA CLK at 460.8 MHz<br>All other combinations are DSIA CLK at 384 MHz. | |
| | 0 | DPPLL_CLK_SRC. This status field indicates the outcome of the clock detection on the REFCLK pin.<br>0 – Clock detected on REFCLK pin. DP_PLL clock derived from input REFCLK (default).<br>1 – No clock detected on REFCLK pin. DP_PLL clock derived from MIPI D-PHY channel A HS continuous clock | | RU |
| 0x0B | 7:0 | Reserved | | R |
| 0x0C | 7:0 | Reserved | | R |
| 0x0D | 0 | DP_PLL_EN<br>When this bit is set, the DP PLL is enabled<br>0 – PLL disabled (default)<br>1 – PLL enabled | | RW |

**Table 25. CSR Bit Field Definitions – DSI Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x10 | 7 | LEFT_RIGHT_PIXELS<br>This bit selects the pixel arrangement in dual channel DSI implementations.<br>0 – DSI channel A receives ODD pixels and channel B receives EVEN (default)<br>1 – DSI channel A receives LEFT image pixels and channel B receives RIGHT image pixels | RW |
| | 6:5 | DSI_CHANNEL_MODE<br>00 – Dual-channel DSI receiver<br>01 – Single channel DSI receiver A (default)<br>10 – Reserved.<br>11 – Reserved | RW |
| | 4:3 | CHA_DSI_LANES<br>This field controls the number of lanes that are enabled for DSI Channel A.<br>00 – Four lanes are enabled<br>01 – Three lanes are enabled<br>10 – Two lanes are enabled<br>11 – One lane is enabled (default)<br>Note: Unused DSI inputs pins on the SN65DSIX6 should be left unconnected. | RW |
| | 2:1 | CHB_DSI_LANES<br>This field controls the number of lanes that are enabled for DSI Channel B.<br>00 – Four lanes are enabled<br>01 – Three lanes are enabled<br>10 – Two lanes are enabled<br>11 – One lane is enabled (default)<br>Note: Unused DSI inputs pins on the SN65DSIX6 should be left unconnected. | RW |
| | 0 | SOT_ERR_TOL_DIS<br>0 – Single bit errors are tolerated for the start of transaction SoT leader sequence (default)<br>1 – No SoT bit errors are tolerated | RW |
| 0x11 | 7:6 | CHA_DSI_DATA_EQ<br>This field controls the equalization for the DSI Channel A Data Lanes<br>00 – No equalization (default)<br>01 – Reserved<br>10 – 1 dB equalization<br>11 – 2 dB equalization | RW |
| | 5:4 | CHB_DSI_DATA_EQ<br>This field controls the equalization for the DSI Channel B Data Lanes<br>00 – No equalization (default)<br>01 – Reserved<br>10 – 1 dB equalization<br>11 – 2 dB equalization | RW |
| | 3:2 | CHA_DSI_CLK_EQ This field controls the equalization for the DSI Channel A Clock<br>00 – No equalization (default)<br>01 – Reserved<br>10 – 1 dB equalization<br>11 – 2 dB equalization | RW |
| | 1:0 | CHB_DSI_CLK_EQ<br>This field controls the equalization for the DSI Channel A Clock<br>00 – No equalization (default)<br>01 – Reserved.<br>10 – 1 dB equalization<br>11 – 2dB equalization | RW |

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**Table 25. CSR Bit Field Definitions – DSI Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x12 | 7:0 | CHA_DSI_CLK_RANGE<br>This field specifies the DSI clock frequency range in 5MHz increments for DSI Channel A clock. The DSIX6 will estimate the DSI clock frequency using the REFCLK frequency determined at the rising edge of EN and update this field accordingly. Software can override this value. . If the CHA_DSI_CLK_RANGE is not loaded before receiving the first DSI packet, the DSIX6 will use the first packet to estimate the DSI_CLK frequency and load this field with this estimate. This first packet may not be received; thus, the host should send a first dummy packet (such as DSI read or write to register 0x00). This field may be written by the host at any time. Any non-zero value written by the host will be used instead of the automatically estimated value.<br>0x00 - 0x07: Reserved<br>0x08 – 40 ≤ frequency < 45 MHz<br>0x09 – 45 ≤ frequency < 50 MHz<br>. . .<br>0x96 – 750 ≤ frequency < 755 MHz<br>0x97 – 0xFF: Reserved | RWU |
| 0x13 | 7:0 | CHB_DSI_CLK_RANGE<br>This field specifies the DSI clock frequency range in 5MHz increments for DSI Channel B clock. The DSIX6 will estimate the DSI clock frequency using the REFCLK frequency determined at the rising edge of EN and update this field accordingly. Software can override this value. If the CHB_DSI_CLK_RANGE is not loaded before receiving the first DSI packet, the DSIX6 will use the first packet to estimate the DSI_CLK frequency and load this field with this estimate. This first packet may not be received; thus, the host should send a first dummy packet (such as DSI read or write to register 0x00). This field may be written by the host at any time. Any non-zero value written by the host will be used instead of the automatically estimated value.<br>0x00 - 0x07: Reserved<br>0x08 – 40 ≤ frequency < 45 MHz<br>0x09 – 45 ≤ frequency < 50 MHz<br>. . .<br>0x96 – 750 ≤ frequency < 755 MHz<br>0x97 – 0xFF: Reserved | RWU |

**Table 26. CSR Bit Field Definitions – Video Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x20 | 7:0 | CHA_ACTIVE_LINE_LENGTH_LOW<br>When the SN65DSIX6 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line for Channel A. When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI channel A. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI channel A. The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00.<br>Note: When the SN65DSIX6 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied. | RW |
| 0x21 | 3:0 | CHA_ACTIVE_LINE_LENGTH_HIGH<br>When the SN65DSIX6 is configured for a single DSI input, this field controls the length in pixels of the active horizontal line for Channel A. When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of odd pixels in the active horizontal line that are received on DSI channel A. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of left pixels in the active horizontal line that are received on DSI channel A. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00.<br>Note: When the SN65DSIX6 is configured for dual DSI inputs in Left/Right mode and LEFT_CROP field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied. | RW |

**Table 26. CSR Bit Field Definitions – Video Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x22 | 7:0 | CHB_ACTIVE_LINE_LENGTH_LOW<br>When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of even pixels in the active horizontal line that are received on DSI channel B. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of right pixels in the active horizontal line that are received on DSI channel B. The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00.<br>Note: When the SN65DSIX6 is configured for dual DSI inputs in Left/Right mode and RIGHT_CROP field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied. | RW |
| 0x23 | 3:0 | CHB_ACTIVE_LINE_LENGTH_HIGH<br>When configured for Dual DSI Inputs in Odd/Even mode, this field controls the number of even pixels in the active horizontal line that are received on DSI channel B. When configured for Dual DSI inputs in Left/Right mode, this field controls the number of right pixels in the active horizontal line that are received on DSI channel B. The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length. This field defaults to 0x00.<br>Note: When the SN65DSIX6 is configured for dual DSI inputs in Left/Right mode and RIGHT_CROP field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied. | RW |
| 0x24 | 7:0 | CHA_VERTICAL_DISPLAY_SIZE_LOW<br>This field controls the vertical display size in lines for Channel A. The value in this field is the lower 8 bits of the 12-bit value for the vertical display size. This field defaults to 0x00. | RW |
| 0x25 | 3:0 | CHA_VERTICAL_DISPLAY_SIZE_HIGH<br>This field controls the vertical display size in lines for Channel A. The value in this field is the upper 4 bits of the 12-bit value for the vertical display size. This field defaults to 0x00. | RW |
| 0x26 – 0x2B | 7:0 | Reserved | R |
| 0x2C | 7:0 | CHA_HSYNC_PULSE_WIDTH_LOW<br>This field controls the width in pixel clocks of the HSync Pulse Width for Channel A. The value in this field is the lower 8-bits of the 15-bit value for HSync Pulse width. This field defaults to 0x00. | RW |
| 0x2D | 7 | CHA_HSYNC_POLARITY.<br>0 – Active High Pulse. Synchronization signal is high for the sync pulse width. (default)<br>1 – Active Low Pulse. Synchronization signal is low for the sync pulse width. | RW |
| | 6:0 | CHA_HSYNC_PULSE_WIDTH_HIGH<br>This field controls the width in pixel clocks of the HSync Pulse Width for Channel A. The value in this field is the upper 7-bits of the 15-bit value for HSync Pulse width. This field defaults to 0x00. | RW |
| 0x2E – 0x2F | 7:0 | Reserved. | R |
| 0x30 | 7:0 | CHA_VSYNC_PULSE_WIDTH_LOW<br>This field controls the length in lines of the VSync Pulse Width for Channel A. . The value in this field is the lower 8-bits of the 15-bit value for VSync Pulse width. This field defaults to 0x00. The total size of the VSYNC pulse width must be at least 1 line. | RW |
| 0x31 | 7 | CHA_VSYNC_POLARITY.<br>0 – Active High Pulse. Synchronization signal is high for the sync pulse width. (Default)<br>1 – Active Low Pulse. Synchronization signal is low for the sync pulse width. | RW |
| | 6:0 | CHA_VSYNC_PULSE_WIDTH_HIGH<br>This field controls the width in lines of the VSync Pulse Width for Channel A. The value in this field is the upper 7-bits of the 15-bit value for VSync Pulse width. This field defaults to 0x00. The total size of the VSYNC pulse width must be at least 1 line. | RW |
| 0x32 – 0x33 | 7:0 | Reserved. | R |
| 0x34 | 7:0 | CHA_HORIZONTAL_BACK_PORCH<br>This field controls the time in pixel clocks between the end of the HSync Pulse and the start of the active video data for Channel A. This field defaults to 0x00. | RW |
| 0x35 | 7:0 | Reserved. | R |

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**Table 26. CSR Bit Field Definitions – Video Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x36 | 7:0 | CHA_VERTICAL_BACK_PORCH<br>This field controls the number of lines between the end of the VSync Pulse and the start of the active video data for Channel A. This field defaults to 0x00. The total size of the Vertical Back Porch must be at least 1 line. | RW |
| 0x37 | 7:0 | Reserved | R |
| 0x38 | 7:0 | CHA_HORIZONTAL_FRONT_PORCH<br>This field controls the time in pixel clocks between the end of the active video data and the start of the HSync Pulse for Channel A. This field defaults to 0x00. | RW |
| 0x39 | 7:0 | Reserved. | R |
| 0x3A | 7:0 | CHA_VERTICAL_FRONT_PORCH<br>This field controls the number of lines between the end of the active video data and the start of the VSync Pulse for Channel A. This field defaults to 0x00. The total size of the Vertical Front Porch must be at least 1 line. | RW |
| 0x3B | 7:0 | Reserved | R |
| 0x3C | 4 | COLOR_BAR_EN. When this bit is set, the SN65DSIX6 will generate a video test pattern on DisplayPort based on the values programmed into the Video Registers for Channel A.<br>0 – Transmit of SMPTE color bar disabled. (default)<br>1 – Transmit of SMPTE color bar enabled. | RW |
| | 3 | Reserved. | R |
| | 2:0 | COLOR_BAR_PATTERN.<br>000 – Vertical Colors: 8 Color (Default)<br>001 – Vertical Colors: 8 Gray Scale<br>010 – Vertical Colors: 3 Color<br>011 – Vertical Colors: Stripes<br>100 – Horizontal Colors: 8 Color<br>101 – Horizontal Colors: 8 Gray Scale<br>110 – Horizontal Colors: 3 Color<br>111 – Horizontal Colors: Stripes | RW |
| 0x3D | 7:0 | RIGHT_CROP. This field controls the number of pixels removed from the beginning of the active video line for DSI Channel B. This field only has meaning if the LEFT_RIGHT_PIXELS = 1. This field defaults to 0x00.<br>Note: When the SN65DSIX6 is configured for dual DSI inputs in Left/Right mode and this field is programmed to a value other than 0x00, the CHB_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Right portion of the line after RIGHT_CROP has been applied. | RW |
| 0x3E | 7:0 | LEFT_CROP. This field controls the number of pixels removed from the end of the active video line for DSI Channel A. This field only has meaning if the LEFT_RIGHT_PIXELS = 1. This field defaults to 0x00.<br>Note: When the SN65DSIX6 is configured for dual DSI inputs in Left/Right mode and this field is programmed to a value other than 0x00, the CHA_ACTIVE_LINE_LENGTH_LOW/HIGH registers must be programmed to the number of active pixels in the Left portion of the line after LEFT_CROP has been applied. | RW |
| 0x3F | 0 | ADEN. This field is used to enable the Assertive Display core for theSN65DSI96. This field has no meaning for the SN65DSI86. Defaults to 0x0 which means the Assertive Display core is disabled. | RW |

**Table 27. CSR Bit Field Definitions – DisplayPort Specific Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x40 | 7:0 | MVID[7:0]. . | RU |
| 0x41 | 7:0 | MVID[15:8] | RU |
| 0x42 | 7:0 | MVID[23:16] | RU |
| 0x43 | 7:0 | NVID[7:0]. | RU |
| 0x44 | 7:0 | NVID[15:8] | RU |
| 0x45 | 7:0 | NVID[23:16] | RU |
| 0x46 | 7:0 | Htotal[7:0]. Defaults to 0x00. | RU |

**Table 27. CSR Bit Field Definitions – DisplayPort Specific Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x47 | 7:0 | Htotal[15:8]. Defaults to 0x00. | RU |
| 0x48 | 7:0 | Vtotal[7:0]. Defaults to 0x00. | RU |
| 0x49 | 7:0 | Vtotal[15:8]. Defaults to 0x00. | RU |
| 0x4A | 7:0 | Hstart[7:0]. Defaults to 0x00. | RU |
| 0x4B | 7:0 | Hstart[15:8]. Defaults to 0x00. | RU |
| 0x4C | 7:0 | Vstart[7:0]. Defaults to 0x00. | RU |
| 0x4D | 7:0 | Vstart[15:8]. Defaults to 0x00. | RU |
| 0x4E | 7:0 | HSW[7:0]. Defaults to 0x00. | RU |
| 0x4F | 7:0 | HSP_HSW[15:8]. Defaults to 0x00. | RU |
| 0x50 | 7:0 | VSW[7:0]. Defaults to 0x00. | RU |
| 0x51 | 7:0 | VSP_VSW[15:8]. Defaults to 0x00. | RU |
| 0x52 | 7:0 | Hwidth[7:0]. Defaults to 0x00. | RU |
| 0x53 | 7:0 | Hwidth[15:8]. Defaults to 0x00. | RU |
| 0x54 | 7:0 | Vheight[7:0]. Defaults to 0x00. | RU |
| 0x55 | 7:0 | Vheight[15:8]. Defaults to 0x00. | RU |
| 0x56 | 7:5 | MSA_MISC0_7_5. This field represents the bits per color.<br>000 – 6 bits per color.<br>001 – 8 bits per color.(Default)<br>Others are not supported. | RU |
| | 4 | MSA_MISC0_4. Defaults to zero. | RW |
| | 3 | MSA_MISC0_3. Defaults to zero. | RW |
| | 2:1 | MSA_MISC0_2_1. This field indicates the format of the data is either RGB, YCbCr(422 or 444). The DSIX6 only supports RGB so this field will always be 0x0.<br>00 – RGB (default) | RU |
| | 0 | MSA_MISC0_0.<br>0 – Link clock and stream clock are async. (default)<br>1 – Link clock and stream clock are sync. | RU |
| 0x57 | 7 | MSA_MISC1_7. Y-only video. The DSIX6 does not support this feature so this field defaults to zero. | R |
| | 6:3 | MSA_MISC1_6_3. Reserved. Default to 0x0. | R |
| | 2:1 | MSA_MISC1_2_1. This field is the stereo video attribute data.<br>00 – No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using SDP called Video Stream Configuration (VSC) packet. (Default)<br>01 – Next frame is Right Eye.<br>10 – Reserved.<br>11 – Next Frame is Left Eye. | RW |
| | 0 | MSA_MISC1_0. Default to zero. | R |
| 0x58 | 7 | TU_SIZE_OVERRIDE. This field is used to control whether DSIX6 determines Transfer Unit Size or the size is determine by the TU_SIZE field.<br>0 – DSIX6 determines TU size. (default)<br>1 – TU size is determined by TU_SIZE field. | RW |
| | 6:0 | TU_SIZE. This field is used to program the DisplayPort transfer Unit size. Valid values are between 32 (0x20) and 64 (0x40). Default is 64. When DSIX6 determines the TU size, the DSIX6 will update this register with the value determined by hardware. SN65DSIX6 will interpret all invalid values to be a transfer unit size of 64 (0x40). | RWU |

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**Table 27. CSR Bit Field Definitions – DisplayPort Specific Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x59 | 7:6 | LN3_ASSIGN. Refer to DP Main Link Configurability section in this document for supported logical to physical combinations based on DP_NUM_LANES.<br>00 – Logical Lane3 is routed to physical ML0P/N pins<br>01 – Logical Lane3 is routed to physical ML1P/N pins<br>10 – Logical Lane3 is routed to physical ML2P/N pins<br>11 – Logical Lane3 is routed to physical ML3P/N pins (default) | RW |
| | 5:4 | LN2_ASSIGN. Refer to DP Main Link Configurability section in this document for supported logical to physical combinations based on DP_NUM_LANES<br>00 – Logical Lane2 is routed to physical ML0P/N pins<br>01 – Logical Lane2 is routed to physical ML1P/N pins<br>10 – Logical Lane2 is routed to physical ML2P/N pins (default)<br>11 – Logical Lane2 is routed to physical ML3P/N pins. | RW |
| | 3:2 | LN1_ASSIGN. Refer to DP Main Link Configurability section in this document for supported logical to physical combinations based on DP_NUM_LANES<br>00 – Logical Lane1 is routed to physical ML0P/N pins<br>01 – Logical Lane1 is routed to physical ML1P/N pins (default)<br>10 – Logical Lane1 is routed to physical ML2P/N pins<br>11 – Logical Lane1 is routed to physical ML3P/N pins. | RW |
| | 1:0 | LN0_ASSIGN. Refer to DP Main Link Configurability section in this document for supported logical to physical combinations based on DP_NUM_LANES.<br>00 – Logical Lane0 is routed to physical ML0P/N pins (default)<br>01 – Logical Lane0 is routed to physical ML1P/N pins<br>10 – Logical Lane0 is routed to physical ML2P/N pins<br>11 – Logical Lane0 is routed to physical ML3P/N pins | RW |
| 0x5A | 7 | ML3_POLR. When this field is set, the polarity of ML3, specified by LN3_ASSIGN, is inverted.<br>0 – ML3 polarity is normal (default)<br>1 – ML3 polarity is inverted. | RW |
| | 6 | ML2_POLR. When this field is set, the polarity of ML2, specified by LN2_ASSIGN, is inverted.<br>0 – ML2 polarity is normal (default)<br>1 – ML2 polarity is inverted. | RW |
| | 5 | ML1_POLR. When this field is set, the polarity of ML1, specified by LN1_ASSIGN, is inverted.<br>0 – ML1 polarity is normal (default)<br>1 – ML1 polarity is inverted. | RW |
| | 4 | ML0_POLR. When this field is set, the polarity of ML0, specified by LN0_ASSIGN, is inverted.<br>0 – ML0 polarity is normal (default)<br>1 – ML0 polarity is inverted. | RW |
| | 3 | VSTREAM_ENABLE. The DSIX6 will clear this field if the following conditions is true: Exiting SUSPEND and the PSR_EXIT_VIDEO bit is cleared.<br>0 – Video data from DSI is not passed to DisplayPort (default). IDLE pattern will be sent instead.<br>1 – Video data from DSI is passed to DisplayPort | RWU |
| | 2 | ENH_FRAME_ENABLE. If AUTHEN_METHOD is Alternate Framing, DSIX6 will automatically enable Enhanced Framing.<br>0 – Disable Enhanced Framing.<br>1 – Enable Enhanced Framing (default) | RWU |
| | 1:0 | Reserved. Defaults to 0x1. | R |
| 0x5B | 1 | ENCH_FRAME_PATT<br>0 – SR BF BF SR or BS BF BF BS (Default)<br>1 – SR CP CP SR or BS CP CP BS | RW |
| | 0 | DP_18BPP_EN. If this field is set, then 18BPP format will be transmitted over eDP interface regardless of the DSI pixel stream datatype format.<br>0 – 24BPP RGB. (default)<br>1 – 18BPP RGB | RW |
| 0x5C | 4 | HPD. Returns the state of the HPD pin after 100ms de-bounce | RU |
| | 0 | HPD_DISABLE<br>0 – HPD input is enabled. (default)<br>1 – HPD input is disabled | RW |

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**Table 28. CSR Bit Field Definitions - GPIO Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x5E | 7 | GPIO4_INPUT. Returns the state of the GPIO4 pin. | RU |
| | 6 | GPIO3_INPUT. Returns the state of the GPIO3 pin. | RU |
| | 5 | GPIO2_INPUT. Returns the state of the GPIO2 pin. | RU |
| | 4 | GPIO1_INPUT. Returns the state of the GPIO1 pin. | RU |
| | 3 | GPIO4_OUTPUT. When GPIO4 Control is programmed to an Output, this field will control the output level of GPIO4.<br>0 – GPIO4 is driven to '0' (GND). (default)<br>1 – GPIO4 is driven to '1'. | RW |
| | 2 | GPIO3_OUTPUT. When GPIO3 Control is programmed to an Output, this field will control the output level of GPIO3.<br>0 – GPIO3 is driven to '0' (GND). (default)<br>1 – GPIO3 is driven to '1'. | RW |
| | 1 | GPIO2_OUTPUT. When GPIO2 Control is programmed to an Output, this field will control the output level of GPIO3.<br>0 – GPIO2 is driven to '0' (GND). (default)<br>1 – GPIO2 is driven to '1'. | RW |
| | 0 | GPIO1_OUTPUT. When GPIO1 Control is programmed to an Output, this field will control the output level of GPIO1.<br>0 – GPIO1 is driven to '0' (GND). (default)<br>1 – GPIO1 is driven to '1'. | RW |
| 0x5F | 7:6 | GPIO4_CTRL<br>00 – Input (Default)<br>01 – Output<br>10 – PWM<br>11 – Reserved. | RW |
| | 5:4 | GPIO3_CTRL<br>00 – Input (Default)<br>01 – Output<br>10 – DSIA HSYNC or VSYNC<br>11 – Reserved | RW |
| | 3:2 | GPI02_CTRL<br>00 – Input (Default)<br>01 – Output<br>10 – DSIA VSYNC<br>11 – Reserved | RW |
| | 1:0 | GPIO1_CTRL<br>00 – Input (Default)<br>01 – Output<br>10 – SUSPEND Input<br>11 – Reserved | RW |

**Table 29. CSR Bit Field Definitions - Native and I2C-Over-Aux Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x60 | 7:1 | I2C_ADDR_CLAIM1. When I2C_CLAIM1_EN is enabled, the DSIX6 will claim I2C slave address programmed into this field. This register defaults to 0x50 which is the typical address for the EDID. | RW |
| | 0 | I2C_CLAIM1_EN<br>0 – Disable (default)<br>1 – Enable | RW |
| 0x61 | 7:1 | I2C_ADDR_CLAIM2. When I2C_CLAIM2_EN is enabled, the DSIX6 will claim I2C slave address programmed into this field. This register defaults to 0x30 which is the default segment pointer register. | RW |
| | 0 | I2C_CLAIM2_EN<br>0 – Disable (Default)<br>1 - Enable | RW |

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**Table 29. CSR Bit Field Definitions - Native and I2C-Over-Aux Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x62 | 7:1 | I2C_ADDR_CLAIM3. When I2C_CLAIM3_EN is enabled, the DSIX6 will claim I2C slave address programmed into this field. This register defaults to 0x52 which is the typical address for the EDID. | RW |
| | 0 | I2C_CLAIM3_EN<br>0 – Disable (Default)<br>1 – Enable | RW |
| 0x63 | 7:1 | I2C_ADDR_CLAIM4. When I2C_CLAIM4_EN is enabled, the DSIX6 will claim I2C slave address programmed into this field. This register defaults to 0x00. | RW |
| | 0 | I2C_CLAIM4_EN<br>0 – Disable (Default)<br>1 - Enable | RW |
| 0x64-0x73 | 7:0 | AUX_WDATA0 thru AUX_WDATA15. Data to transmit. All of these registers default to 0x00. | RW |
| 0x74 | 7:4 | Reserved | R |
| | 3:0 | AUX_ADDR[19:16]. This field is address bits 19 thru 16 of the Native Aux 20-bit address. This field shall be filled with zeros for I2C-Over-Aux transitions. This field defaults to 0x0. | RW |
| 0x75 | 7:0 | AUX_ADDR[15:8]. This field is bits 15 thru 8 of the Native Aux 20-bit address. This field shall be filled with zeros for I2C-Over-Aux request transactions. This field defaults to 0x00. | RW |
| 0x76 | 7:0 | AUX_ADDR[7:0]. This field is address bits 7 thru 0 of the Native Aux 20-bit address. For I2C-Over-Aux request transactions this field shall be the 7-bit I2C address. This field defaults to 0x00. | RW |
| 0x77 | 4:0 | AUX_LENGTH. Amount of Data to transmit or amount of data received. Limited to up to 16 bytes. For example, if LENGTH is 0x10, then DSIX6 will interpret this to mean 16 (0x10). For replies, DSIX6 will update this field with the number of bytes returned. This field defaults to 0x00. | RWU |
| 0x78 | 7:4 | AUX_CMD. This field is used to indicate the type of request. This field defaults to 0x00. Refer to Table 13 for request transactions codes. | RW |
| | 0 | SEND. When set to a '1', the DSIX6 will send the Native Aux request or initiate the I2C-Over_Aux transaction. DSIX6 will clear this bit when the request completed successfully or failed due to an error. This field defaults to 0. | RSU |
| 0x79 – 0x88 | 7:0 | AUX_RDATA0 thru AUX_RDATA15. Data received. All of these registers default to 0x00. | RU |

**Table 30. CSR Bit Field Definitions – Link Training Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x89 – 0x92 | 7:0 | 80BIT_CUSTOM_PATTERN.<br>These 10 bytes represent the 80-bit Custom pattern. The default pattern is 0x1F, 0x7C, 0xF0, 0xC1, 0x07, 0x1F, 0x7C, 0xF0, 0xC1, and 0x07. In the DisplayPort PHY CTS specification this pattern is known as PLTPAT. The SN65DSIX6 will continuously transmit over all enabled DisplayPort lanes starting at the the lsb of data at address 0x89 through the msb of data at address 0x92 last. | RW |

**Table 30. CSR Bit Field Definitions – Link Training Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x93 | 7:6 | DP_PRE_EMPHASIS<br>This field selects the pre-emphasis setting for all DP Main Links. The actual pre-emphasis level is determined by the DP Link Training LUT registers.<br>00 – Pre-Emphasis Level 0 (Default)<br>01 – Pre-Emphasis Level 1<br>10 – Pre-Emphasis Level 2<br>11 – Pre-Emphasis Level 3 | RWU |
| | 5:4 | DP_NUM_LANES.<br>00 - Not Configured. (Default)<br>01 - 1 DP lane.<br>10 - 2 DP lanes.<br>11 - 4 DP lanes. | RW |
| | 3:1 | SSC_SPREAD<br>000 – Down-spread 5000 ppm<br>001 – Down-spread 4375 ppm<br>010 – Down-spread 3750 ppm (default)<br>011 – Down-spread 3150 ppm<br>100 – Down-spread 2500 ppm<br>101 – Center-spread 3750 ppm<br>110 – Center-spread 4375 ppm<br>111 – Center-spread 5000 ppm | RW |
| | 0 | SSC_ENABLE<br>0 – Clock spread is disabled (default)<br>1 – Clock spread is enabled. | RW |
| 0x94 | 7:5 | DP_DATARATE<br>000 – Not Configured (Default)<br>001 – 1.62Gbps per lane (RBR)<br>010 – 2.16Gbps per lane<br>011 – 2.43Gbps per lane<br>100 - 2.70Gbps per lane (HBR)<br>101 – 3.24Gbps per lane<br>110 – 4.32Gbps per lane.<br>111 - 5.4Gbps per lane (HBR2) | RW |
| | 3:2 | DP_ERC. This field controls the edge rate for Main Link DisplayPort interface.<br>00 – 45 to 50 ps (default)<br>01 – 59.6 to 78 ps<br>10 – 83 to 117 ps<br>11 – 109 to 146 ps. | RW |
| | 1:0 | DP_TX_SWING<br>This field selects the differential output voltage level for all DP Main Links. The actual pk-pk differential tx voltage is determined by the *DP Link Training LUT registers*. Note that Voltage Swing level 3 is disabled by default.<br>00 – Voltage Swing Level 0 (Default)<br>01 – Voltage Swing Level 1<br>10 – Voltage Swing Level 2<br>11 – Voltage Swing Level 3 | RWU |

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**Table 30. CSR Bit Field Definitions – Link Training Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0x95 | 7 | TPS1_FAST_TRAIN.<br>0 – TPS1 will not be transmitted in Fast Link Training Mode (Default)<br>1 – TPS1 will be transmitted in Fast Link Training Mode | RW |
| | 6 | TPS2_FAST_TRAIN<br>0 – TPS2 will NOT be transmitted in Fast Link Training mode (default)<br>1 – TPS2 will be transmitted in Fast Link Training Mode | RW |
| | 5 | TPS3_FAST_TRAIN<br>0 – TPS3 will not be used for TPS2 in Fast Link Training Mode (default)<br>1 – TPS3 will be used instead of TPS2 in Fast Link Training Mode. | RW |
| | 4 | SCRAMBLE_DISABLE<br>0 – Scrambling Enabled (default)<br>1 – Scrambling Disabled. | RW |
| | 3:1 | DP_POST_CURSOR2. This field contains the post cursor2 value, where PST2 = 20 * LOG(1 – 0.05 * DP_POST_CURSOR2) (in dB)<br>This field controls the Post Cursor2 is setting for all DP Main Links<br>000 – Post-Cursor2 Level 0 (0 dB) (Default)<br>010 – Post-Cursor2 Level 1 (0.92 dB)<br>100 – Post-Cursor2 Level 2 (1.94 dB)<br>110 – Post-Cursor2 Level 3 (3.10 dB). | RWU |
| | 0 | ADJUST_REQUEST_DISABLE. This field is used during Semi-Auto Link training.<br>0 – DSIX6 will read from DPCD address to determine next training level (pre-emphasis, tx swing level, and post-cursor2). (Default)<br>1 – DSIX6 will not read from DPCD address to determine next training level. It will instead go to next available Pre-emphasis level. After max pre-emphasis level has been reached, the DSIX6 will attempt next DP_TX_SWING and reset pre-emphasis level back to level 0. Post-Cursor2 is not used in this mode. | RW |
| 0x96 | 3:0 | ML_TX_MODE<br>0000 – Main Link Off (default)<br>0001 – Normal mode (Idle pattern or active video)<br>0010 – TPS1<br>0011 – TPS2<br>0100 – TPS3<br>0101 – PRBS7<br>0110 – HBR2 Compliance Eye Pattern<br>0111 – Symbol Error Rate Measurement Pattern<br>1000 – 80 bit Custom Pattern<br>1001 – Fast Link Training<br>1010 – Semi Auto Link Training.<br>1011 – Redriver Semi Auto Link Training<br>All others – Reserved. | RWU |
| 0x97 | 7:0 | HBR2_COMPEYEPAT_LENGTH_LOW. This field is the count of number of scrambled 0 symbols to be output for every Enhanced Framing Scrambler Reset sequence. This count includes the reset sequence. A value less than four causes scrambled 0 symbols to be output with no scrambler reset sequence. This field represents the lower 8 bits of the 16-bit HBR2_COMPEYEPAT_LENGTH register. This field defaults to 0x04. | RW |
| 0x98 | 7:0 | HBR2_COMPEYEPAT_LENGTH_HIGH. This field is the count of number of scrambled 0 symbols to be output for every Enhanced Framing Scrambler Reset sequence. This count includes the reset sequence. A value less than four causes scrambled 0 symbols to be output with no scrambler reset sequence. This field represents the upper 8 bits of the 16-bit HBR2_COMPEYEPAT_LENGTH register. This field defaults to 0x01. | RW |
| 0x99 | 7 | LINK_RATE_SET_EN. When this field is cleared, the Semi-Auto Link training will write the appropriate value (0x06 for 1.62Gbps, 0x0A for 2.7Gbps, or 0x14 for 5.4Gbps) to the sink's LINK_BW_SET register at DPCD address 0x00110. When this field is set, the Semi-Auto Link Training will write the value in the LINK_RATE_SET field to the sink's LINK_RATE_SET register at DPCD address 0x00115. Defaults to 0. | RW |
| | 2:0 | LINK_RATE_SET. When LINK_RATE_SET_EN bit is set, the value in this field will be written to the sink's LINK_RATE_SET register at DPCD address 0x00115 during Semi-Auto Link training process. Defaults to 0x0. | RW |

**Table 31. CSR Bit Field Definitions – PWM Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xA0 | 7:0 | PWM_PRE_DIV<br>The value programmed into this field along with the value in BACKLIGHT_SCALE is used to set the PWM frequency. The PWM frequency = REFCLK / (PWM_PRE_DIV * BACKLIGHT_SCALE + 1). This field defaults to 0x01 | RW |
| 0xA1 | 7:0 | BACKLIGHT_SCALE_LOW.<br>The digital value corresponding to the maximum possible backlight input value. Default to 0xFF. The value in this field is the lower 8 bits of the 16-bit BACKLIGHT_SCALE register. | RW |
| 0xA2 | 7:0 | BACKLIGHT_SCALE_HIGH.The digital value corresponding to the maximum possible backlight input value. Default to 0xFF. The value in this field is the upper 8 bits of the 16-bit BACKLIGHT scale register. | RW |
| 0xA3 | 7:0 | BACKLIGHT_LOW<br>Screen brightness on a scale of 0 to BACKLIGHT_SCALE. This register is used for SN65DSI86. This register is also used for SN65DSI96 when OPTION_SELECT is not equal to zero. The value in this field is the lower 8 bits of the 16-bit BACKLIGHT register. Defaults to 0x00 | RW |
| 0xA4 | 7:0 | BACKLIGHT_HIGH<br>Screen brightness on a scale of 0 to BACKLIGHT_SCALE. This register is used for SN65DSI86. This register is also used for SN65DSI96 when OPTION_SELECT is not equal to zero. The value in this field is the upper 8 bits of the 16-bit BACKLIGHT register. Default to 0x00. The DSIX6 will latch the 16-bit BACKLIGHT value on a write to this field. | RW |
| 0xA5 | 1 | PWM_EN.<br>0 – PWM is disabled. (Default).<br>1 – PWM enabled. | RW |
| | 0 | PWM_INV. When this bit is set, the PWM output will be inverted.<br>0 – Normal (default)<br>1 – Inverted. | RW |

**Table 32. CSR Bit Field Definitions – DP Link Training LUT**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xB0 | 7:4 | V0_P0_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V0_P0_PRE) (in dB), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 0 are select by the training algorithm. The default value for this field is 0 (0 dB). | RW |
| | 3:0 | V0_P0_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V0_P0_VOD (in mV), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 0 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 4 (400mV). | RW |
| 0xB1 | 7:4 | V0_P1_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V0_P1_PRE) (in dB), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 1 are select by the training algorithm. The default value for this field is 7 (3.74 dB). | RW |
| | 3:0 | V0_P1_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V0_P1_VOD (in mV), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 1 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 8 (600mV). | RW |
| 0xB2 | 7:4 | V0_P2_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V0_P2_PRE) (in dB), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 2 are select by the training algorithm. The default value for this field is 10 (6.02 dB). | RW |
| | 3:0 | V0_P2_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V0_P2_VOD (in mV), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 2 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |

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**Table 32. CSR Bit Field Definitions – DP Link Training LUT (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xB3 | 7:4 | V0_P3_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V0_P3_PRE) (in dB), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 3 are select by the training algorithm. The default value for this field is 10 (6.02 dB). | RW |
| | 3:0 | V0_P3_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V0_P3_VOD (in mV), when the DP_TX_SWING = Level 0 and DP_PRE_EMPHASIS = Level 3 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xB4 | 7:4 | V1_P0_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V1_P0_PRE) (in dB), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 0 are select by the training algorithm. The default value for this field is 0 (0 dB). | RW |
| | 3:0 | V1_P0_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V1_P0_VOD (in mV), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 0 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 8 (600mV). | RW |
| 0xB5 | 7:4 | V1_P1_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V1_P1_PRE) (in dB), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 1 are select by the training algorithm. The default value for this field is 6 (3.10 dB). | RW |
| | 3:0 | V1_P1_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V1_P1_VOD (in mV), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 1 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xB6 | 7:4 | V1_P2_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V1_P2_PRE) (in dB), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 2 are select by the training algorithm. The default value for this field is 9 (5.19 dB). | RW |
| | 3:0 | V1_P2_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V1_P2_VOD (in mV), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 2 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xB7 | 7:4 | V1_P3_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V1_P3_PRE) (in dB), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 3 are select by the training algorithm. The default value for this field is 9 (5.19 dB). | RW |
| | 3:0 | V1_P3_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V1_P3_VOD (in mV), when the DP_TX_SWING = Level 1 and DP_PRE_EMPHASIS = Level 3 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xB8 | 7:4 | V2_P0_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V2_P0_PRE) (in dB), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 0 are select by the training algorithm. The default value for this field is 0 (0 dB). | RW |
| | 3:0 | V2_P0_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V2_P0_VOD (in mV), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 0 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xB9 | 7:4 | V2_P1_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V2_P1_PRE) (in dB), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 1 are select by the training algorithm. The default value for this field is 5 (2.50 dB). | RW |
| | 3:0 | V2_P1_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V2_P1_VOD (in mV), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 1 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |

**Table 32. CSR Bit Field Definitions – DP Link Training LUT (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xBA | 7:4 | V2_P2_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V2_P2_PRE) (in dB), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 2 are select by the training algorithm. The default value for this field is 5 (2.50 dB). | RW |
| | 3:0 | V2_P2_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V2_P2_VOD (in mV), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 2 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xBB | 7:4 | V2_P3_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V2_P3_PRE) (in dB), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 3 are select by the training algorithm. The default value for this field is 5 (2.50 dB). | RW |
| | 3:0 | V2_P3_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V2_P3_VOD (in mV), when the DP_TX_SWING = Level 2 and DP_PRE_EMPHASIS = Level 3 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xBC | 7:4 | V3_P0_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V3_P0_PRE) (in dB), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 0 are select by the training algorithm. The default value for this field is 0 (0 dB). | RW |
| | 3:0 | V3_P0_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V3_P0_VOD (in mV), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 0 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xBD | 7:4 | V3_P1_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V3_P1_PRE) (in dB), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 1 are select by the training algorithm. The default value for this field is 0 (0 dB). | RW |
| | 3:0 | V3_P1_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V3_P1_VOD (in mV), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 1 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xBE | 7:4 | V3_P2_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V3_P2_PRE) (in dB), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 2 are select by the training algorithm. The default value for this field is 0 (0 dB). | RW |
| | 3:0 | V3_P2_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V3_P2_VOD (in mV), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 2 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |
| 0xBF | 7:4 | V3_P3_PRE. This field contains the post1 pre-emphasis code, where the pre-emphasis setting is given by PREdB = -20 * LOG(1 – 0.05 * V3_P3_PRE) (in dB), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 3 are select by the training algorithm. The default value for this field is 0 (0 dB). | RW |
| | 3:0 | V3_P3_VOD. This field contains the TX swing code, where the emphasized output pk-pk differential voltage is given by VOD = 200 + 50 * V3_P3_VOD (in mV), when the DP_TX_SWING = Level 3 and DP_PRE_EMPHASIS = Level 3 are selected by the training algorithm. The maximum supported value is 12 (800mV). Any value greater than 12 is reserved for SN65DSIX6. The default value for this field is 12 (800mV). | RW |

**Table 32. CSR Bit Field Definitions – DP Link Training LUT (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xC0 | 7 | V0_P3_PRE_EN. When this field is set V0_P3_PRE is used in training algorithm. When this field is cleared, V0_P3_PRE is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 6 | V0_P3_VOD_EN. When this field is set V0_P3_VOD is used in training algorithm. When this field is cleared, V0_P3_VOD is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 5 | V0_P2_PRE_EN. When this field is set V0_P2_PRE is used in training algorithm. When this field is cleared, V0_P2_PRE is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 4 | V0_P2_VOD_EN. When this field is set V0_P2_VOD is used in training algorithm. When this field is cleared, V0_P2_VOD is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 3 | V0_P1_PRE_EN. When this field is set V0_P1_PRE is used in training algorithm. When this field is cleared, V0_P1_PRE is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 2 | V0_P1_VOD_EN. When this field is set V0_P1_VOD is used in training algorithm. When this field is cleared, V0_P1_VOD is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 1 | V0_P0_PRE_EN. When this field is set V0_P0_PRE is used in training algorithm. When this field is cleared, V0_P0_PRE is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 0 | V0_P0_VOD_EN. When this field is set V0_P0_VOD is used in training algorithm. When this field is cleared, V0_P0_VOD is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| 0xC1 | 7 | V1_P3_PRE_EN. When this field is set V1_P3_PRE is used in training algorithm. When this field is cleared, V1_P3_PRE is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 6 | V1_P3_VOD_EN. When this field is set V1_P3_VOD is used in training algorithm. When this field is cleared, V1_P3_VOD is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 5 | V1_P2_PRE_EN. When this field is set V1_P2_PRE is used in training algorithm. When this field is cleared, V1_P2_PRE is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 4 | V1_P2_VOD_EN. When this field is set V1_P2_VOD is used in training algorithm. When this field is cleared, V1_P2_VOD is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 3 | V1_P1_PRE_EN. When this field is set V1_P1_PRE is used in training algorithm. When this field is cleared, V1_P1_PRE is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 2 | V1_P1_VOD_EN. When this field is set V1_P1_VOD is used in training algorithm. When this field is cleared, V1_P1_VOD is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 1 | V1_P0_PRE_EN. When this field is set V1_P0_PRE is used in training algorithm. When this field is cleared, V1_P0_PRE is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 0 | V1_P0_VOD_EN. When this field is set V1_P0_VOD is used in training algorithm. When this field is cleared, V1_P0_VOD is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| 0xC2 | 7 | V2_P3_PRE_EN. When this field is set V2_P3_PRE is used in training algorithm. When this field is cleared, V2_P3_PRE is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 6 | V2_P3_VOD_EN. When this field is set V2_P3_VOD is used in training algorithm. When this field is cleared, V2_P3_VOD is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 5 | V2_P2_PRE_EN. When this field is set V2_P2_PRE is used in training algorithm. When this field is cleared, V2_P2_PRE is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 4 | V2_P2_VOD_EN. When this field is set V2_P2_VOD is used in training algorithm. When this field is cleared, V2_P2_VOD is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 3 | V2_P1_PRE_EN. When this field is set V2_P1_PRE is used in training algorithm. When this field is cleared, V2_P1_PRE is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 2 | V2_P1_VOD_EN. When this field is set V2_P1_VOD is used in training algorithm. When this field is cleared, V2_P1_VOD is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 1 | V2_P0_PRE_EN. When this field is set V2_P0_PRE is used in training algorithm. When this field is cleared, V2_P0_PRE is not used in training algorithm. The default for this field is 1 (enabled). | RW |
| | 0 | V2_P0_VOD_EN. When this field is set V2_P0_VOD is used in training algorithm. When this field is cleared, V2_P0_VOD is not used in training algorithm. The default for this field is 1 (enabled). | RW |

**Table 32. CSR Bit Field Definitions – DP Link Training LUT (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xC3 | 7 | V3_P3_PRE_EN. When this field is set V3_P3_PRE is used in training algorithm. When this field is cleared, V3_P3_PRE is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 6 | V3_P3_VOD_EN. When this field is set V3_P3_VOD is used in training algorithm. When this field is cleared, V3_P3_VOD is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 5 | V3_P2_PRE_EN. When this field is set V3_P2_PRE is used in training algorithm. When this field is cleared, V3_P2_PRE is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 4 | V3_P2_VOD_EN. When this field is set V3_P2_VOD is used in training algorithm. When this field is cleared, V3_P2_VOD is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 3 | V3_P1_PRE_EN. When this field is set V3_P1_PRE is used in training algorithm. When this field is cleared, V3_P1_PRE is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 2 | V3_P1_VOD_EN. When this field is set V3_P1_VOD is used in training algorithm. When this field is cleared, V3_P1_VOD is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 1 | V3_P0_PRE_EN. When this field is set V3_P0_PRE is used in training algorithm. When this field is cleared, V3_P0_PRE is not used in training algorithm. The default for this field is 0 (disabled). | RW |
| | 0 | V3_P0_VOD_EN. When this field is set V3_P0_VOD is used in training algorithm. When this field is cleared, V3_P0_VOD is not used in training algorithm. The default for this field is 0 (disabled). | RW |

**Table 33. CSR Bit Field Definitions – PSR Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xC8 | 1 | PSR_EXIT_VIDEO.<br>0 – Upon exiting SUSPEND mode, the DSIX6 will transmit IDLE patterns and the VSTREAM_ENABLE bit will be cleared. GPU software is responsible for setting the VSTREAM_ENABLE bit. (default)<br>1 – Upon exiting SUSPEND mode, the DSIX6 will transmit IDLE patterns and the VSTREAM_ENABLE bit will be set. | RW |
| | 0 | PSR_TRAIN. This field controls whether or not the DSIX6 will perform a Semi-Auto Link Training when exiting the SUSPEND mode.<br>0 – PSR train will be Normal Mode (idle pattern) (default)<br>1 – PSR train will be Semi-Auto Link Training. | RW |

**Table 34. CSR Bit Field Definitions – IRQ Enable Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xE0 | 0 | IRQ_EN<br>When enabled by this field, the IRQ output is driven high to communicate IRQ events.<br>0 – IRQ output is high-impedance (default)<br>1 – IRQ output is driven high when a bit is set in registers 0xF0, 0xF1, 0xF2, 0xF3, 0xF4, or 0xF5 that also has the corresponding IRQ_EN bit set to enable the interrupt condition | RW |

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**Table 34. CSR Bit Field Definitions – IRQ Enable Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xE1 | 7 | CHA_CONTENTION_DET_EN<br>0 – CHA_CONTENTION_DET_ERR is masked (default)<br>1 – CHA_CONTENTION_DET_ERR is enabled to generate IRQ events | RW |
| | 6 | CHA_FALSE_CTRL_EN<br>0 – CHA_FALSE_CTRL_ERR is masked (default)<br>1 – CHA_FALSE_CTRL_ERR is enabled to generate IRQ events | RW |
| | 5 | CHA_TIMEOUT_EN<br>0 – CHA_TIMEOUT_ERR is masked (default)<br>1 – CHA_TIMEOUT_ERR is enabled to generate IRQ events | RW |
| | 4 | CHA_LP_TX_SYNC_EN<br>0 – CHA_LP_TX_SYNC_ERR is masked (default)<br>1 – CHA_LP_TX_SYNC_ERR is enabled to generate IRQ events | RW |
| | 3 | CHA_ESC_ENTRY_EN<br>0 – CHA_ESC_ENTRY_ERR is masked (default)<br>1 – CHA_ESC_ENTRY_ERR is enabled to generate IRQ events | RW |
| | 2 | CHA_EOT_SYNC_EN<br>0 – CHA_EOT_SYNC_ERR is masked (default)<br>1 – CHA_EOT_SYNC_ERR is enabled to generate IRQ events | RW |
| | 1 | CHA_SOT_SYNC_EN<br>0 – CHA_SOT_SYNC_ERR is masked (default)<br>1 – CHA_SOT_SYNC_ERR is enabled to generate IRQ events | RW |
| | 0 | CHA_SOT_BIT_EN<br>0 – CHA_SOT_BIT_ERR is masked (default)<br>1 – CHA_SOT_BIT_ERR is enabled to generate IRQ events | RW |
| 0xE2 | 7 | CHA_DSI_PROTOCOL_EN<br>0 – CHA_DSI_PROTOCOL_ERR is masked (default)<br>1 – CHA_DSI_PROTOCOL_ERR is enabled to generate IRQ events | RW |
| | 6 | Reserved | R |
| | 5 | CHA_INVALID_LENGTH_EN<br>0 – CHA_INVALID_LENGTH_ERR is masked (default)<br>1 – CHA_INVALID_LENGTH_ERR is enabled to generate IRQ events | RW |
| | 4 | Reserved. | R |
| | 3 | CHA_DATATYPE_EN<br>0 – CHA_DATATYPE_ERR is masked (default)<br>1 – CHA_ DATATYPE_ERR is enabled to generate IRQ events | RW |
| | 2 | CHA_CHECKSUM_EN<br>0 – CHA_CHECKSUM_ERR is masked (default)<br>1 – CHA_CHECKSUM_ERR is enabled to generate IRQ events | RW |
| | 1 | CHA_UNC_ECC_EN<br>0 – CHA_UNC_ECC_ERR is masked (default)<br>1 – CHA_UNC_ECC_ERR is enabled to generate IRQ events | RW |
| | 0 | CHA_COR_ECC_EN<br>0 – CHA_COR_ECC_ERR is masked (default)<br>1 – CHA_COR_ECC_ERR is enabled to generate IRQ events | RW |

**Table 34. CSR Bit Field Definitions – IRQ Enable Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xE3 | 7 | Reserved | R |
| | 6 | CHB_FALSE_CTRL_EN<br>0 – CHB_FALSE_CTRL_ERR is masked (default)<br>1 – CHB_FALSE_CTRL_ERR is enabled to generate IRQ events | RW |
| | 5 | Reserved. | R |
| | 4 | CHB_LP_TX_SYNC_EN<br>0 – CHB_LP_TX_SYNC_ERR is masked (default)<br>1 – CHB_LP_TX_SYNC_ERR is enabled to generate IRQ events | RW |
| | 3 | Reserved | R |
| | 2 | CHB_EOT_SYNC_EN<br>0 – CHB_EOT_SYNC_ERR is masked (default)<br>1 – CHB_EOT_SYNC_ERR is enabled to generate IRQ events | RW |
| | 1 | CHB_SOT_SYNC_EN<br>0 – CHB_SOT_SYNC_ERR is masked (default)<br>1 – CHB_SOT_SYNC_ERR is enabled to generate IRQ events | RW |
| | 0 | CHB_SOT_BIT_EN<br>0 – CHB_SOT_BIT_ERR is masked (default)<br>1 – CHB_SOT_BIT_ERR is enabled to generate IRQ events | RW |
| 0xE4 | 7 | CHB_DSI_PROTOCOL_EN<br>0 – CHB_DSI_PROTOCOL_ERR is masked (default)<br>1 – CHB_DSI_PROTOCOL_ERR is enabled to generate IRQ events | RW |
| | 6 | Reserved | R |
| | 5 | CHB_INVALID_LENGTH_EN<br>0 – CHB_INVALID_LENGTH_ERR is masked (default)<br>1 – CHB_INVALID_LENGTH_ERR is enabled to generate IRQ events | RW |
| | 4 | Reserved | R |
| | 3 | CHB_DATATYPE_EN<br>0 – CHB_DATATYPE_ERR is masked (default)<br>1 – CHB_ DATATYPE_ERR is enabled to generate IRQ events | RW |
| | 2 | CHB_CHECKSUM_EN<br>0 – CHB_CHECKSUM_ERR is masked (default)<br>1 – CHB_CHECKSUM_ERR is enabled to generate IRQ events | RW |
| | 1 | CHB_UNC_ECC_EN<br>0 – CHB_UNC_ECC_ERR is masked (default)<br>1 – CHB_UNC_ECC_ERR is enabled to generate IRQ events | RW |
| | 0 | CHB_COR_ECC_EN<br>0 – CHB_COR_ECC_ERR is masked (default)<br>1 – CHB_COR_ECC_ERR is enabled to generate IRQ events | RW |

**Table 34. CSR Bit Field Definitions – IRQ Enable Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xE5 | 7 | I2C_DEFR_EN<br>0 – I2C_DEFR is masked (default)<br>1 – I2C_DEFR is enabled to generate IRQ events. | RW |
| | 6 | NAT_I2C_FAIL_EN.<br>0 – NAT_I2C_FAIL is masked. (default)<br>1 – NAT_I2C_FAIL is enabled to generate IRQ events. | RW |
| | 5 | AUX_SHORT_EN<br>0 – AUX_SHORT is masked. (default)<br>1 – AUX_SHORT is enabled to generate IRQ events. | RW |
| | 4 | AUX_DEFR_EN.<br>0 – AUX_DEFR is masked. (default)<br>1 – AUX_DEFR is enabled to generate IRQ events. | RW |
| | 3 | AUX_RPLY_TOUT_EN.<br>0 – AUX_RPLY_TOUT is masked (default).<br>1 – AUX_RPLY_TOUT is enabled to generate IRQ events. | RW |
| | 2 | Reserved. | R |
| | 1 | Reserved. | R |
| | 0 | SEND_INT_EN.<br>0 – SEND_INT is masked (default)<br>1 – SEND_INT is enabled to generate IRQ events. | RW |
| 0xE6 | 7 | BL_OUT_CHANGE_EN. This field is only meaningful for SN65DSI96.<br>0 – BL_OUT_CHANGE is masked (default)<br>1 – BL_OUT_CHANGE is enabled to generate IRQ events. | RW |
| | 6 | AD_PWR_STATUS_EN. This field is only meaningful for SN65DSI96<br>0 – AD_PWR_STATUS is masked (default)<br>1 – AD_PWR_STATUS is enabled to generate IRQ events | RW |
| | 5 | PLL_UNLOCK_EN<br>0 – PLL_UNLOCK is masked (default)<br>1 – PLL_UNLOCK is enabled to generate IRQ events | RW |
| | 4 | CALC_DONE_EN. This field only applies to theSN65DSI96.<br>0 – CALC_DONE is masked (default)<br>1 – CALC_DONE is enabled to generate IRQ events | RW |
| | 3 | HPD_REPLUG_EN.<br>0 – HPD_REPLUG is masked (default)<br>1 – HPD_REPLUG is enabled to generate IRQ events | RW |
| | 2 | HPD_REMOVAL _EN<br>0 – HPD_REMOVAL is masked. (default)<br>1 – HPD_REMOVAL is enabled to generate IRQ events. | RW |
| | 1 | HPD_INSERTION_EN<br>0 – HPD_INSERTION is masked. (default)<br>1 – HPD_INSERTION is enabled to generate IRQ events. | RW |
| | 0 | IRQ_HPD_EN<br>0 – IRQ_HPD is masked. (default)<br>1 – IRQ_HPD is enabled to generate IRQ events. | RW |

**Table 34. CSR Bit Field Definitions – IRQ Enable Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xE7 | 7 | DPTL_VIDEO_WIDTH_PROG_ERR_EN<br>0 – DPTL_VIDEO_WIDTH_PROG_ERR is masked. (default)<br>1 – DPTL_VIDEO_WIDTH_PROG_ERR is enabled to generate IRQ events. | RW |
| | 6 | DPTL_LOSS_OF_DP_SYNC_LOCK_EN<br>0 – DPTL_LOSS_OF_DP_SYNC_LOCK_ERR is masked. (default)<br>1 – DPTL_LOSS_OF_DP_SYNC_LOCK_ERR is enabled to generate IRQ events. | RW |
| | 5 | DPTL_UNEXPECTED_DATA_EN<br>0 – DPTL_UNEXPECTED_DATA_ERR is masked. (default)<br>1 – DPTL_UNEXPECTED_DATA_ERR is enabled to generate IRQ events. | RW |
| | 4 | DPTL_UNEXPECTED_SECDATA_EN<br>0 – DPTL_UNEXPECTED_SECDATA_ERR is masked. (default)<br>1 – DPTL_UNEXPECTED_SECDATA_ERR is enabled to generate IRQ events. | RW |
| | 3 | DPTL_UNEXPECTED_DATA_END_EN<br>0 – DPTL_UNEXPECTED_DATA_END_ERR is masked. (default)<br>1 – DPTL_UNEXPECTED_DATA_END_ERR is enabled to generate IRQ events. | RW |
| | 2 | DPTL_UNEXPECTED_PIXEL_DATA_EN<br>0 – DPTL_UNEXPECTED_PIXEL_DATA_ERR is masked. (default)<br>1 – DPTL_UNEXPECTED_PIXEL_DATA_ERR is enabled to generate IRQ events. | RW |
| | 1 | DPTL_UNEXPECTED_HSYNC_EN<br>0 – DPTL_UNEXPECTED_HSYNC_ERR is masked. (default)<br>1 – DPTL_UNEXPECTED_HSYNC_ERR is enabled to generate IRQ events. | RW |
| | 0 | DPTL_UNEXPECTED_VSYNC_EN<br>0 – DPTL_UNEXPECTED_VSYNC_ERR is masked. (default)<br>1 – DPTL_UNEXPECTED_VSYNC_ERR is enabled to generate IRQ events. | RW |
| 0xE8 | 7 | STRENGTH_OUT_CHANGE_EN. This field is only meaningful for SN65DSI96.<br>0 – STRENGTH_OUT_CHANGE is masked. (default)<br>1 – STRENGTH_OUT_CHANGE is enabled to generate IRQ events. | RW |
| | 1 | DPTL_SECONDARY_DATA_PACKET_PROG_ERR_EN.<br>0 – DPTL_SECONDARY_DATA_PACKET_PROG_ERR is masked. (default)<br>1 – DPTL_SECONDARY_DATA_PACKET_PROG_ERR is enabled to generate IRQ events. | RW |
| | 0 | DPTL_DATA_UNDERRUN_EN<br>0 – DPTL_DATA_UNDERRUN_ERR is masked. (default)<br>1 – DPTL_DATA_UNDERRUN_ERR is enabled to generate IRQ events. | RW |
| 0xE9 | 7:6 | Reserved. | R |
| | 5 | LT_EQ_CR_ERR_EN.<br>0 – LT_EQ_CR_ERR is masked (default)<br>1 – LT_EQ_CR_ERR is enabled to generate IRQ events. | RW |
| | 4 | LT_EQ_LPCNT_ERR_EN.<br>0 – LT_EQ_LPCNT_ERR is masked (default)<br>1 – LT_EQ_LPCNT_ERR is enabled to generate IRQ events. | RW |
| | 3 | LT_CR_MAXVOD_ERR_EN.<br>0 – LT_CR_MAXVOD_ERR is masked (default)<br>1 – LT_CR_MAXVOD_ERR is enabled to generate IRQ events. | RW |
| | 2 | LT_CR_LPCNT_ERR_EN.<br>0 – LT_CR_LPCNT_ERR is masked (default)<br>1 – LT_CR_LPCNT_ERR is enabled to generate IRQ events. | RW |
| | 1 | LT_FAIL_EN.<br>0 – LT_FAIL is masked (default)<br>1 – LT_FAIL is enabled to generate IRQ events. | RW |
| | 0 | LT_PASS_EN.<br>0 – LT_PASS is masked (default)<br>1 – LT_PASS is enabled to generate IRQ events. | RW |

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**Table 35. CSR Bit Field Definitions – IRQ Status Registers**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xF0 | 7 | CHA_CONTENTION_DET_ERR. When LP high or LP low fault is detected on the DSI channel A interface, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 6 | CHA_FALSE_CTRL_ERR. When the DSI channel A packet processor detects a LP Request not followed by the remainder of a valid escape or turnaround sequence or if it detects a HS request not followed by a bridge state (LP-00), this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 5 | CHA_TIMEOUT_ERR. When the HS Rx Timer or the LP TX timer expires, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 4 | CHA_LP_TX_SYNC_ERR. When the DSI channel A packet processor detects data not synchronized to a byte boundary at the end of Low-Power transmission, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 3 | CHA_ESC_ENTRY_ERR. When the DSI Channel A packet processor detects an unrecognized Escape Mode Entry Command, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 2 | CHA_EOT_SYNC_ERR. When the DSI channel A packet processor detects that the last byte of a HS transmission does not match a byte boundary, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 1 | CHA_SOT_SYNC_ERR. When the DSI channel A packet processor detects a corrupted SOT in a way that proper synchronization cannot be expected, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 0 | CHA_SOT_BIT_ERR When the DSI channel A packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| 0xF1 | 7 | CHA_DSI_PROTOCOL_ERR. When the DSI channel A packet processor detects a DSI protocol error, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 6 | Reserved. | R |
| | 5 | CHA_INVALID_LENGTH_ERR. When the DSI channel A packet processor detects an invalid transmission length, this bit is set; this bit is cleared by writing a’1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 4 | Reserved. | R |
| | 3 | CHA_DATATYPE_ERR. When the DSI channel A packet processor detects a unrecognized DSI data type, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 2 | CHA_CHECKSUM_ERR When the DSI channel A packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 1 | CHA_UNC_ECC_ERR When the DSI channel A packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |
| | 0 | CHA_COR_ECC_ERR When the DSI channel A packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a ‘1’ value or when the DSIX6 responds to a Generic read/write request or unsolicited BTA with a Acknowledge and Error Report. | RCU |

**Table 35. CSR Bit Field Definitions – IRQ Status Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xF2 | 7 | Reserved | R |
| | 6 | CHB_FALSE_CTRL_ERR. When the DSI channel B packet processor detects a LP Request not followed by the remainder of a valid escape or turnaround sequence or if it detects a HS request not followed by a bridge state (LP-00), this bit is set; this bit is cleared by writing a '1' value. | RCU |
| | 5 | Reserved | R |
| | 4 | CHB_LP_TX_SYNC_ERR. When the DSI channel B packet processor detects data not synchronized to a byte boundary at the end of Low-Power transmission, this bit is set; this bit is cleared by writing a '1' value. | RCU |
| | 3 | Reserved | R |
| | 2 | CHB_EOT_SYNC_ERR. When the DSI channel B packet processor detects that the last byte of a HS transmission does not match a byte boundary, this bit is set; this bit is cleared by writing a '1' value. | RCU |
| | 1 | CHB_SOT_SYNC_ERR. When the DSI channel B packet processor detects a corrupted SOT in a way that proper synchronization cannot be expected, this bit is set; this bit is cleared by writing a '1' value. | RCU |
| | 0 | CHB_SOT_BIT_ERR When the DSI channel B packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a '1' value. | RCU |
| 0xF3 | 7 | CHB_DSI_PROTOCOL_ERR. When the DSI channel B packet processor detects a DSI protocol error, this bit is set; this bit is cleared by writing a '1' value. | RCU |
| | 6 | Reserved. | R |
| | 5 | CHB_INVALID_LENGTH_ERR. When the DSI channel B packet processor detects an invalid transmission length, this bit is set; this bit is cleared by writing a'1' value. | RCU |
| | 4 | Reserved. | R |
| | 3 | CHB_DATATYPE_ERR. When the DSI channel B packet processor detects a unrecognized DSI data type, this bit is set; this bit is cleared by writing a '1' value. | RCU |
| | 2 | CHB_CHECKSUM_ERR When the DSI channel B packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a '1'. | RCU |
| | 1 | CHB_UNC_ECC_ERR When the DSI channel B packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a '1' value. | RCU |
| | 0 | CHB_COR_ECC_ERR When the DSI channel B packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a '1' value. | RCU |
| 0xF4 | 7 | I2C_DEFR. This field is set if an I2C-Over-Aux request has received a specific number X of I2C_DEFER from Sink. For direct method (clock stretching), the number X is 44. For indirect method, the number X is 44 for AUX_LENGTH = 1, 66 for AUX_LENGTH = 2, 110 for 2 < AUX_LENGTH ≤ 4, 154 for 4 < AUX_LENGTH ≤ 6, 198 for 6< AUX_LENGTH ≤ 8, 287 for 8< AUX_LENGTH ≤ 12, and 375 for 12 < AUX_LENGTH ≤ 16. | RCU |
| | 6 | NAT_I2C_FAIL. This bit is set if the I2C-Over-Aux or Native AUX failed. | RCU |
| | 5 | AUX_SHORT. If set, then the bytes written or received did not match requested Length. SW should read AUX_LENGTH field to determine the amount of data written or read. | RCU |
| | 4 | AUX_DEFR. The DSIX6 will attempt to complete an AUX request by retrying the request seven times. This field is set if the response to the last retry is an AUX_DEFER. | RCU |
| | 3 | AUX_RPLY_TOUT. The DSIX6 will attempt to complete an AUX request by retrying the request seven times. This field is set if the response to the last retry is a 400-us timeout. | RCU |
| | 2 | Reserved. | R |
| | 1 | Reserved. | R |
| | 0 | SEND_INT. This field is set whenever the SEND bit transitions from 1 to 0. | RCU |
| 0xF5 | 7 | BL_OUT_CHANGE. This field is set whenever the BACKLIGHT_OUT field changes from a previously reported value. This field only has meaning for the SN65DSI96. | RCU |
| | 6 | AD_PWR_STATUS. This field is set when the Assertive Display core is powered on after the ADEN bit is set. This field only has meaning for the SN65DSI96. | RCU |
| | 5 | PLL_UNLOCK This bit is set whenever the PLL Lock status transitions from LOCK to UNLOCK. | RCU |
| | 4 | CALC_DONE. This field is set whenever the Assertive Display parameter calculation is completed. This field only applies to the SN65DSI96. | RCU |
| | 3 | HPD_REPLUG. This field is set whenever the DSIX6 detects a replug event on the HPD pin. | RCU |
| | 2 | HPD_REMOVAL. This field is set whenever the DSIX6 detects a DisplayPort device removal. | RCU |
| | 1 | HPD_INSERTION. This field is set whenever the DSIX6 detects a DisplayPort device insertion. | RCU |
| | 0 | IRQ_HPD. This field is set whenever the DSIX6 detects a IRQ_HPD event. | RCU |

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**Table 35. CSR Bit Field Definitions – IRQ Status Registers (continued)**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xF6 | 7 | VIDEO_WIDTH_PROG_ERR. This field is set whenever the video parameters define more bytes of pixel data than can be transferred in the allotted video portion of the line time. | RCU |
| | 6 | LOSS_OF_DP_SYNC_LOCK_ERR. This field is set whenever the DP sync generator has lost lock with the DSI sync stream. | RCU |
| | 5 | DPTL_UNEXPECTED_DATA_ERR. This field is set whenever a data token at in the video stream from DSI was found at an invalid time syntactically. | RCU |
| | 4 | DPTL_UNEXPECTED_SECDATA_ERR. This field is set whenever a secondary data start token at in the video stream was found at an invalid time syntactically. | RCU |
| | 3 | DPTL_UNEXPECTED_DATA_END_ERR. This field is set whenever a data end token at in the video stream from DSI was found at an invalid time syntactically. | RCU |
| | 2 | DPTL_UNEXPECTED_PIXEL_DATA_ERR. This field is set whenever a video data start token at in the video stream from DSI was found at an invalid time syntactically. | RCU |
| | 1 | DPTL_UNEXPECTED_HSYNC_ERR. This field is set whenever a horizontal sync token at in the video stream from DSI was found at an invalid time syntactically. | RCU |
| | 0 | DPTL_UNEXPECTED_VSYNC_ERR. This field is set whenever a vertical sync token at in the video stream from DSI was found at an invalid time syntactically. | RCU |
| 0xF7 | 7 | STRENGTH_OUT_CHANGE. This field is set whenever the STRENGTH_OUT changes. This field is only meaningful for SN65DSI96. | RCU |
| | 1 | DPTL_SECONDARY_DATA_PACKET_PROG_ERR. This field is set whenever a secondary data packet has an invalid length. | RCU |
| | 0 | DPTL_DATA_UNDERRUN_ERR. This field is set whenever no data was received when data should have been ready. | RCU |
| 0xF8 | 7:6 | Reserved. | R |
| | 5 | LT_EQ_CR_ERR. This field is set whenever link training fails in the channel equalization phase due to LANEx_CR_DONE not set. | RCU |
| | 4 | LT_EQ_LPCNT_ERR. This field is set whenever link training fails in the channel equalization phase due to the loop count being greater than five. | RCU |
| | 3 | LT_CR_MAXVOD_ERR. This field is set whenever link training fails in clock recovery phase due to max VOD reached without LANEx_CR_DONE bit(s) getting set. | RCU |
| | 2 | LT_CR_LPCNT_ERR. This field is set whenever link training fails in the clock recovery phase due to same VOD being used five times. | RCU |
| | 1 | LT_FAIL. This field is set whenever the Semi-Auto link training fails to train the DisplayPort Link. | RCU |
| | 0 | LT_PASS. This field is set whenever the Semi-Auto link training successfully trains the DisplayPort Link. | RCU |

**Table 36. Page Select Register**

| ADDRESS | BIT(S) | DESCRIPTION | ACCESS |
|---|---|---|---|
| 0xFF | 2:0 | PAGE_SELECT. This field is used to select a different page of 254 bytes. This register will reside in the same location for each Page. This register is independently controlled by either DSI or I2C. This means the value written or read by I2C does not affect the value written or read by DSI, or vice-versa. The SN65DSI86 can only access Page 0 and Page 7.<br>000 – Standard CFR registers. (Default)<br>001 – Assertive Display CFR Registers<br>010 – Assertive Display's Calibration Lookup Table (AL_CALIB_LUT)<br>011 – Assertive Display's Asymmetry Function Lookup Table (LUT_FI)<br>100 – Assertive Display's Color Correction Lookup Table (LUT_CC)<br>101 – Reserved.<br>110 – Assertive Display's Post Gamma Lookup Table (post_gamma_lut)<br>111 – TI Test Registers. | RW |

# APPLICATION INFORMATION

## Typical Implementation

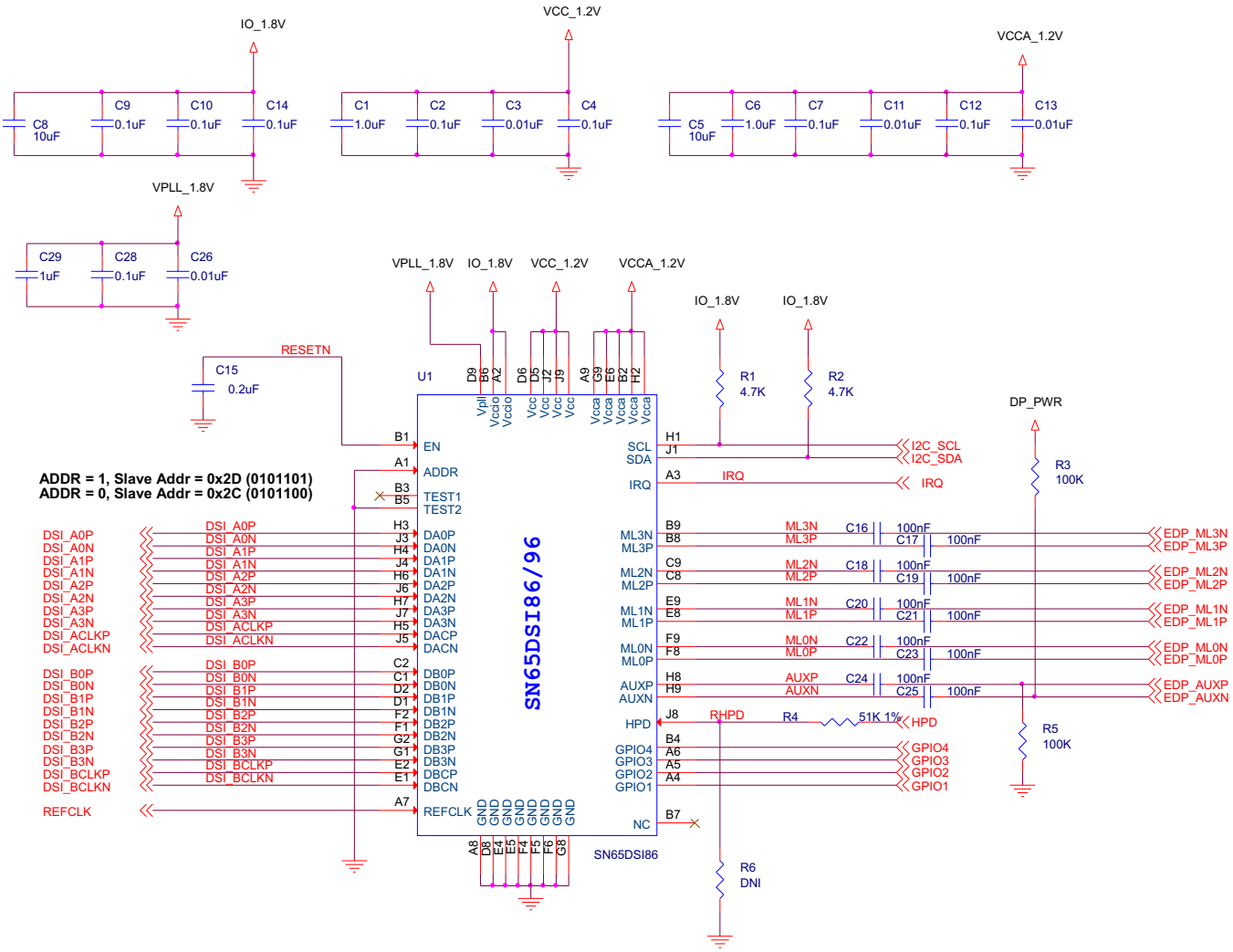



**Figure 18. Typical Implementation**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65DSI86ZQER | PREVIEW | BGA MICROSTAR JUNIOR | ZQE | 64 | 2500 | TBD | Call TI | Call TI | -40 to 85 | | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

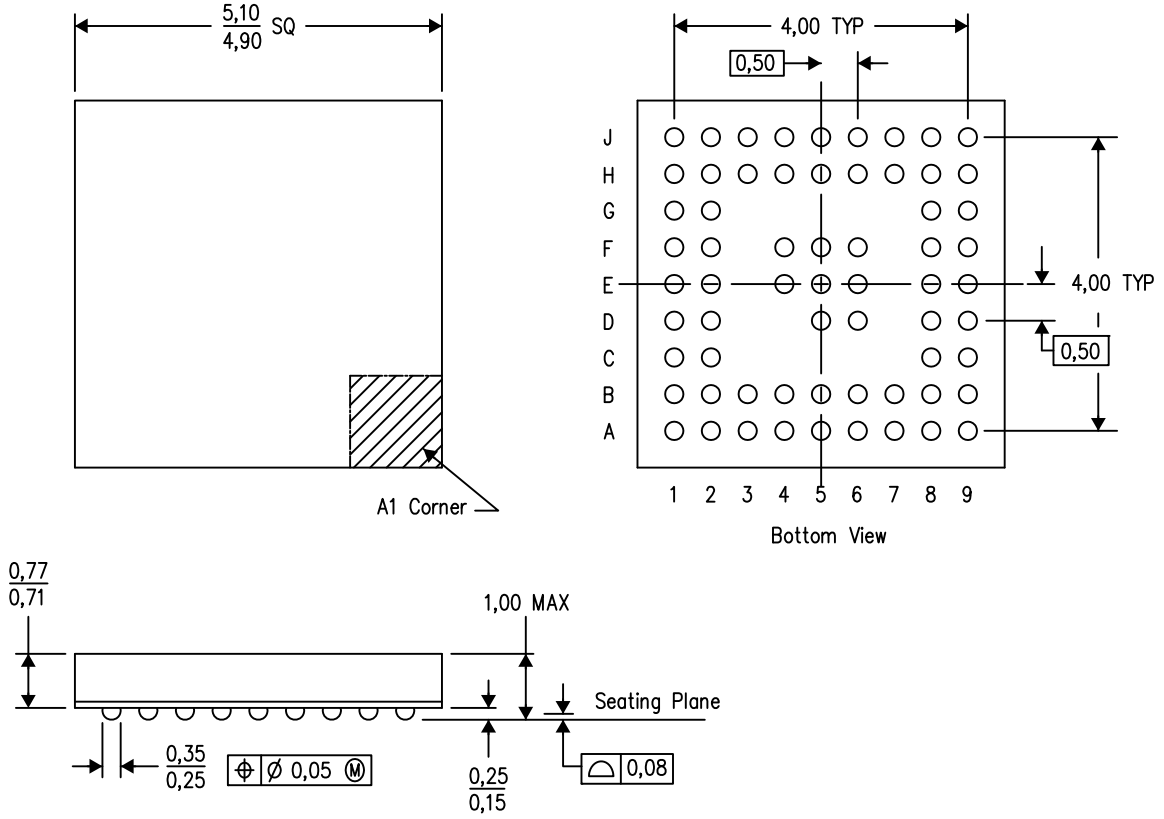
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

ZQE (S–PBGA–N64) PLASTIC BALL GRID ARRAY

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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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